ALD Applications
Room Tampa Bay Salons 5-9 - Session AA-TuP
ALD Applications Poster Session

AA-TuP-1 Improving the Thermoelectric Properties of ALD Synthesized Thermoelectric Thin Films Sb_2Te_3 by Cr+ and Ar+Ion Implantation, *Sadiya Tahsin,* ***Helmut Baumgart,*** Old Dominion University

Atomic layer deposition (ALD) provides atomic-scale thickness control and excellent conformality, enabling the integration of thermoelectric materials onto complex, high–aspect ratio architectures. In this study, Sb_2Te_3 thin films were deposited by ALD on planar and porous silicon substrates and subsequently modified through ion implantation to independently tune electrical and thermal transport. Chromium (Cr^+) and argon (Ar^+) ions were employed to decouple chemical doping from structural disorders. Cr^+ implantation was used to adjust carrier concentration through electrically active doping, while Ar^+ implantation introduced lattice defects and disorder without chemical substitution. Post-implantation annealing at 225 °C enabled partial defect recovery and dopant activation. Hall effect measurements reveal a substantial increase in carrier concentration and electrical conductivity in annealed, implanted films compared to pristine as-deposited samples. This enhancement is accompanied by reduced carrier mobility, consistent with increased carrier scattering from implantation-induced defects. These results demonstrate that combining ALD-enabled conformal growth with controlled ion-beam defect engineering offers a scalable pathway for optimizing Sb_2Te_3 thermoelectric thin films through independent control of electronic and phononic transport.

AA-TuP-2 A New Sn-based Precursor as Dry Photoresist for Extreme Ultraviolet Lithography Process , ***Junsok Choi****, Shijin Song, Youngwon Kim, Juhyung Lee, Ahreum Kim, Seonghan Kim, Dae Won Ryu,* Hansol Chemical, Republic of Korea

Extreme Ultraviolet Lithography (EUVL) has become essential process for reduction in device dimension. Recently, in EUVL, Dry-deposition & Dry-development approaches have attracted considerable attention because of their capability of preventing pattern collapse, relaxing Resolution-Line edge roughness-Sensitivity (RLS) trade-off, and reducing environment effect. As Photoresists (PR) for Dry EUVL, Sn-based precursors with EUV-sensitive ligands have been widely researched due to high absorption coefficient of Sn towards EUV light.

In this study, we developed a new Sn precursor as a dry PR for EUVL. The thin PR films of 25 nm were deposited through chemical vapor deposition (CVD). Then, 5X5 μm^2 patterns and 1:1 line/space (L/S) patterns were formed through E-beam lithography process for measurement of sensitivity resolution and line-edge roughness (LER) of the developed dry PR.

The sensitivity of the dry PR was evaluated with E-beam dose when thickness after development reaches maximum with increasing the dose for 5X5 μm^2 patterns. The thickness of those patterns after development were measured through optical microscopy. D_{100} (Dose at maximum thickness) of the PR was 399 $\mu C/cm^2$ at the voltage of 100 kV.

1:1 L/S patterns with half pitch = 50, 40, 30, 20, and 10 nm were observed with scanning electron microscopy (SEM). From hp = 50 nm to hp = 20 nm, no major defects (pattern collapse, bridging and line pinching) was observed. LER at hp =20 nm measured with Lacern program was only 1.66 nm. These results showed that our developed dry PR has satisfactory performances to realize ultra-fine nano-patterns for reducing dimension of semiconductor devices.

AA-TuP-3 Development of Air-stable Liquid Niobium Precursor with Organic-inorganic Hybrid Ligand for Conformal Atomic Layer Deposition of Nb_2O_5, ***Sun Young Baik****, Sangbum Han,* EGTM, Republic of Korea

Metal halide precursors are widely used in Atomic Layer Deposition (ALD) and Chemical Vapor Deposition (CVD) due to their high reactivity with common oxygen sources and exceptional thermal stability. These characteristics enable excellent conformality and often produce high-purity films with lower carbon and oxygen contamination compared to many organometallic precursors. However, despite their effectiveness, a notable limitation is that most metal halides exist in the solid phase, which complicates precursor delivery and necessitates the use of specialized canisters. Additionally, corrosive reaction byproducts (e.g., HF, HCl) can damage ALD chamber components. To address these limitations, we developed a novel niobium (Nb) precursor by combining halide and organic ligands. This new Nb precursor synergizes the advantages of both ligand types; it retains the reactivity of halides while exhibiting exceptional air stability and existing in the liquid phase at room temperature. Notably, the precursor demonstrated excellent properties during the deposition process. Its liquid state facilitates stable delivery, and its superior thermal stability allows for deposition at higher temperatures. Consequently, the precursor was confirmed to achieve perfect step coverage (~100%) on patterned wafers, comparable to that of conventional metal halide precursors. We expect this new Nb precursor to be a suitable candidate for the ALD of Nb2O5 interfacial oxide layers.

AA-TuP-4 ZnO Thin Film Transistor-Based Hydrogen Sensor Fabricated by Atomic Layer Deposition, *Kaito Otsuka, Kyosuke Nakazawa, Ryo Miyazawa, Masanori Miura, Bashir Ahmmad,* ***Fumihiko Hirose****,* Graduate School of Science and Engineering, Yamagata University, Japan

Hydrogen sensors are crucial devices for securing hydrogen based power generation systems. As the conventional technologies, palladium nanoparticle films were used as measuring its resistance as the H_2 signal. Moreover, the transparent oxide semiconductors such as ZnO were used as the sensing resistor for hydrogen. On the other hand, thin–film–transistor (TFT)–based sensors are attracting increasing attention because a TFT matrix can be used as a two–dimensional sensing platform. In the present study, ZnO–based TFT sensors were fabricated by atomic layer deposition to explore their potential for hydrogen detection.

In Fig. 1, the schematic of the TFT is illustrated. A nanometer–thick (12 nm) ZnO film was used as the channel layer, and the thickness was minimized to enhance the sensitivity. The ZnO film was deposited by room–temperature atomic layer deposition. The deposition system is shown in Fig. 2. The precursors were dimethylzinc and plasma–excited humidified argon. The deposition temperature was room temperature. The film was then annealed in dry air at 450°C for 30min to promote crystallization. In this TFT, the channel length and width were 60μm and 1mm, respectively.

For the hydrogen sensing test, we measured the time variation of the drain current with gate and drain voltages of 0 and 20V, respectively. The hydrogen partial pressure was increased stepwise from 200 to 6400Pa. The drain current clearly increased with increasing partial pressure, although no saturation was observed. It was also confirmed that the slope of the drain–current response correlated with the partial pressure, suggesting the applicability of the present device as a hydrogen sensor. We assume that hydrogen molecules were adsorbed on the palladium oxide, dissociated into atomic hydrogen, and diffused into the ZnO channel, where the enhanced carrier conduction led to the steep increase in drain current.

At the conference, we will discuss the operation mechanism together with more detailed experimental results.

AA-TuP-5 Titanium Nitride Protective Coatings for High-Performance Proton Exchange Membrane Water Electrolysis, ***Bhavesh Chavan****, Ruud Kortlever, Ruud van Ommen,* Delft University of Technology, Netherlands

Proton-exchange membrane (PEM) water electrolysis is a leading technology for green hydrogen production, offering high efficiency and compact design. However, its widespread adoption is hindered by the reliance on costly platinum group metals and titanium-based components required to endure the acidic, oxidizing environment during operation [1].

Titanium-based components, such as the porous transport layer (PTL) and bipolar plates, play critical roles in facilitating mass transport, ensuring uniform current and heat distribution, and providing mechanical stability to the system. Yet, under operational conditions, these components form semiconducting oxide layers, which reduce electrical conductivity and compromise system efficiency. Additionally, they require high hydrophilicity to improve gas-liquid contact and mass transfer. To address these challenges, these components are often coated with thick layers (~200nm) of precious metals such as platinum or gold, increasing costs significantly [2].

In this work, titanium nitride (TiN) coatings are investigated as a cost-effective alternative to conventional Pt or Au coatings on PTLs, aiming to provide high corrosion resistance, conductivity, and hydrophilicity [3,4]. Three gas-phase coating techniques to make TiN are explored in this work: atomic layer deposition (ALD), reactive sputtering (physical vapor deposition), and direct plasma nitridation. ALD offers excellent coating conformality and high penetration depth but involves a more complex and time-intensive process. In contrast, reactive sputtering is a simpler and more cost-effective method, though it can compromise coating conformality. The conformality achievable with direct plasma nitridation remains uncertain and requires further evaluation.

Initial studies involved TiN film deposition on silicon wafers to evaluate coating quality, followed by application on 3D PTL structures. Electrochemical testing was first conducted in a three-electrode setup, after

which the coated PTLs were evaluated under PEM water electrolysis conditions. The results of our work demonstrate the potential of titanium nitride coatings as a scalable protective layer for PEM water electrolysis components, offering a pathway toward cost-effective and efficient green hydrogen production.

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AA-TuP-6 Controlled Interface Oxidation of Ru/RuO_2 Thin Films Through High Concentration H_2O_2 Exposure*, Austen Adams, Dan Le,* ***Walter Hernandez****,* RASIRC

The modern trend of semiconductor device design approaching increasingly smaller scales, alongside the desire for devices to be integrated into complex three-dimensional architectures, has caused an industry-wide need for precise control over film quality and interface properties. The interface between bottom electrode materials and dielectric layers is of particular interest as the thickness of a modern dielectric decreases to the single nanometer range. Ru is a well-studied bottom electrode material for dynamic random-access memory applications, in part due to its low bulk resistivity (7.1 μΩ cm) and high work function (4.7eV). Unfortunately, during oxidation cycles of dielectric ALD the industry standard O_3 exposure often causes the formation of volatile RuO_4. The result of this oxidation effect being lower quality Ru-based interfaces with etched RuO_2. In previous semiconductor generations this surface roughness for a bottom electrode interface would be a minor concern, but as modern semiconductor designs demand thinner films, the need for a higher quality and uniform interfaces has become pertinent.

Here we showcase evidence of higher quality uniform RuO_2 thin film formation via BRUTE Peroxide (high concentration H_2O_2)exposure, mitigating the formation of RuO_4. We compare these films to comparable O_3 exposed Ru/RuO_2 films and as-deposited Ru films. Resulting structures are characterized through scanning electron microscopy surface imaging, x-ray reflectivity and x-ray photoelectron spectroscopy analysis, among other techniques.

AA-TuP-7 Plasma-Enhanced Atomic Layer Deposition of Niobium Nitride Using a New Nb Precursor and Its Application to Diffusion Barriers for Cu and Ru Interconnects*, Kyungmin Kim,* Department of Energy and Chemical Engineering, Ulsan National Institute of Science and Technology (UNIST), Republic of Korea*; Chaehyun Park, Minjeong Kweon,* Graduate School of Semiconductor Materials and Devices Engineering, Ulsan National Institute of Science and Technology (UNIST), Republic of Korea*; Yongjoo Park, Donghyun Kim,* Advanced Reasearch Development Team, SK Trichem Co. Ltd., Sejong, 30068, Korea*; Soo-Hyun Kim,* Graduate School of Semiconductor Materials and Devices Engineering, Ulsan National Institute of Science and Technology (UNIST), Department of Materials Science and Engineering, Ulsan National Institute of Science and Technology (UNIST), Republic of Korea

Continued scaling of semiconductor interconnects has led to increased RC delay, reduced Cu volume, size-effect-induced resistivity increase, and degraded electromigration reliability. Conventional Cu interconnects rely on complex TaN/Ta diffusion barrier and liner stacks. However, this multilayer scheme faces severe scaling limitations, thereby motivating the search for alternative diffusion barrier and liner materials. Transition-metal nitrides (TMNs) especially niobium nitride (NbN) offer high melting point (≈2400 °C), strong chemical stability, and metallic conductivity (58–78 μΩ·cm), making them suitable diffusion barrier candidates for advanced interconnect integration [1] [2]. As interconnect dimensions continue to shrink, atomic layer deposition (ALD) becomes essential due to its self-limiting surface reactions, excellent conformality, and precise thickness control in high-aspect-ratio device structures. In this study, we investigate the ALD feasibility of NbN_x thin films using a novel liquid Nb precursor, which offers higher volatility and stable vapor delivery compared with conventional solid precursors such as $NbCl_5$ or NbF_5. Multiple reactants including NH_3 molecule, NH_3 plasma, N_2 plasma, and N_2:H_2 mixture plasma were examined to identify effective nitridation pathways. Among them, NH_3 plasma was the only reactant capable of forming crystalline NbN_x and further experiments were done mainly using NH_3 plasma. The ALD-NbN_x process was conducted in a showerhead-type PEALD reactor (IOV dX1 PEALD, ISAC RESEARCH, Korea). Self-limiting growth behavior was confirmed through both precursor and reactant pulsing time, with a saturated growth rate of approximately 0.18 Å/cycle. A stable ALD temperature window was identified between 250–350 °C, with the best film quality achieved at 300 °C. The properties of ALD-grown NbN_x films were characterized using XRD, XRR, SEM, XPS and TEM. Finally, the ALD-grown NbN_x films were evaluated as diffusion barrier for Cu and Ru interconnects, demonstrating their potential for advanced interconnect applications. Detailed barrier performance results will be presented at the conference.

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Acknowledgements

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AA-TuP-8 Ultrathin Sn-Doped In_2O_3 Films for Scalable Semiconductor Transistors*, Seung Ho Ryu, Seong Keun Kim,* Korea University, Republic of Korea*; Taikyu Kim,* Stanford University, Republic of Korea*; Taeseok Kim,* Korea University, Republic of Korea

As transistor scaling progresses, ultrathin channel structures are increasingly required to suppress short-channel effects and enhance gate control in advanced device architectures such as FinFETs and gate-all-around (GAA) transistors. However, reducing channel thickness typically leads to severe degradation in conductivity, limiting the electrical performance of thin-film transistors (TFTs). In this study, we investigate an ultrathin Sn-doped In_2O_3 (ITO) channel to overcome this challenge. The uniform Sn doping enhances carrier density and mitigates the conductivity degradation associated with ultrathin channels, ensuring stable electrical performance. As a result, we successfully fabricate enhancement-mode TFTs with a 1.5 nm-thick ITO channel, achieving a high field-effect mobility of 33.4 ± 1.5 $cm^2/V{\cdot}s$, a subthreshold swing of 129 ± 30 mV/dec, and a threshold voltage of 0.3 V. These findings provide a crucial strategy for realizing high-performance oxide TFTs with ultrathin conducting channels, addressing a key challenge in the development of next-generation semiconductor devices.

AA-TuP-9 A Film-Quality-Aware ALD Integration Framework for Top-Gated MoS_2 FETs*, Minjong Lee, Thi Thu Huong Chu, Inhong Hwang, Doo San Kim, Dushyant Narayan, Dan Le, Soham Shirodkar, Jiyoung Kim,* University of Texas at Dallas

Top-gated MoS_2 FETs require conformal, ultrathin high-k dielectrics with low interface trap density [1]. However, the surface-limited reactions in atomic layer deposition (ALD) can also perturb MoS_2 channel chemistry, degrading electrostatic control and limiting reproducibility [2]. It is thus critical to establish a process-channel framework that decouples nucleation-driven interface formation from channel-damaging reactions. In this work, we examine how MoS_2 film quality governs top-gate insulator integration and defines the boundary between chemistry-enabled interface improvement and defect-activated channel damage.

We first established a single-crystal benchmark using mechanically exfoliated few-layer MoS_2. Comparative oxidant studies show that H_2O_2-based ALD of HfO_2 yields improved gate controllability relative to conventional oxidants (H_2O, O_3), consistent with a chemically stabilized interface associated with S-O bond formation. These results indicate that oxidant engineering can overcome the conventional nucleation-interface-quality tradeoff without relying on seed or interfacial-layer strategies, providing a practical route for scaled top-gated 2D devices.

We then extend the same gate-stack process to wafer-scale MoS_2 films from multiple sources (e.g., chemical vapor deposition (CVD)- and chemical vapor transfer (CVT)-grown). In contrast to exfoliated single-crystal flakes, large-area MoS_2 exhibits overall degradation after high-k deposition, indicating that film non-idealities and spatial variability dominate the integration outcome. We attribute this divergence to defect-mediated interfacial chemistry, where abundant reactive sites in wafer-scale MoS_2

promote localized oxidation and non-ideal bonding even under H_2O_2-enabled deposition, thereby degrading transport and gate controllability. This trend further suggests that defective MoS_2 films require milder ALD windows (e.g., lower temperature and reduced oxidant reactivity) to suppress defect-activated parasitic reactions while preserving nucleation.

Overall, this study establishes process-structure-property relationships linking MoS2 quality to top-gate dielectric integration and provides actionable design rules for reliable 2D FET gate stacks toward future 3D-integrated electronics.

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AA-TuP-10 Atomic Layer Deposition of Pt on Plasma-Activated Tungsten Oxide Support for Durable PEMFC Anodes, ***Hyung Jong Choi***, Stanford University*; Hae Wook Park, Beum Geun Seo, Jung Woo Shim, Nam Il Kim, Yun Sung Choi,* Korea University, Republic of Korea*; Fritz B. Prinz,* Stanford University*; Joon Hyung Shim,* Korea University, Republic of Korea

Atomic layer deposition (ALD) can provide a unique pathway to maximize the utilization of noble metal catalysts by controlling the distribution and loading at the nanoscale. This study fabricated Pt nanoparticles on WO3 support using plasma-enhanced ALD (PEALD) to develop a high-performance anode catalyst for polymer electrolyte membrane fuel cells (PEMFCs) operated under fuel starvation conditions. Prior to Pt deposition, the surface of the WO3 support was treated by Ar plasma to generate oxygen vacancies and enhance the electrical conductivity of the support. The surface treatment could accelerate Pt island formation on the WO3 surface, which is driven by activation of the WO3 surface. The resulting Pt–WO3 interface could enhance hydrogen spillover and form HxWO3 species, which can act as a temporary proton–electron buffer via reversible decomposition, which is helpful in fuel starvation situations. The species also helps consume intruding oxygen during start-up/shutdown, thereby stabilizing the anode potential. As a result, the resulting catalyst platform fabricated by Ar plasma treatment and the subsequent PEALD Pt process showed enhanced stability compared to commercial Pt/C across multiple harsh protocols, including fuel-starvation transients.

AA-TuP-12 High-quality CeO_2 thin films by low temperature atomic layer deposition using a new heteroleptic Ce precursor, ***Juri Kim***, *Yewon Seo, Soo-Hyun Kim,* Ulsan National Institute of Science and Technology (UNIST), Republic of Korea

Cerium oxide (CeO_2) is a rare-earth oxide with a high dielectric constant, moderate bandgap, excellent chemical stability, and multiple valence states (Ce^{3+}/Ce^{4+}). Owing to these properties, CeO_2 has been widely investigated for applications such as CMOS gate dielectrics, SOFCs, gas sensors, and resistive switching memories. The formation of CeO_2 requires complete oxidation of Ce^{3+} to Ce^{4+}, which demands a relatively high oxidation potential. However, under low-temperature ALD conditions,the limited oxidation capability of conventional O_2- and H_2O-based oxidants often results in degraded film quality due to incomplete oxidation and residual organic species.To overcome these limitations, O_3 was selected as the oxidant in this study. Ozone (O_3) generates highly reactive oxygen species upon decomposition, providing strong oxidation capability and enabling effective low-temperature oxidation without plasma assistance. In this work, CeO_2 films were deposited by ALD (IOV dX1 PEALD reactor, ISAC Research, Korea) using aheterolepticcyclopentadienyl-amidinate Ce precursor and O_3 as the reactant. As shown in Figure 1, CeO_2 films deposited using O_3 exhibit stronger diffraction peaks than those grown with conventional oxidants (H_2O, O_2, and O_2 plasma), indicating improved crystallinity. The deposition temperature was conducted at temperatures ranging from 150 to 350 °C, with 200 °C determined as the optimal growth temperature. The self-limiting growth behavior was shown with both precursor pulsing and reactant pulsing and the saturated growth-per-cycle (GPC) was approximately 1.15 Å/cycle. Film properties varied with deposition conditions and were characterized by SEM (thickness), TEM (step coverage, thickness), XRR (density and thickness), XRD (crystallinity), XPS (composition) and RBS (impurity). Electrical properties were evaluated via Metal–Oxide–Semiconductor capacitors, focusing on dielectric constant and leakage current. The detailed results will be presented at the conference.

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AA-TuP-13 Drain-Current-Enhanced TiO_2-Thin-Film Transistors Fabricated by Atomic Layer Deposition, ***Ryo Miyazawa***, *Tsubasa Takami, Masanori Miura, Bashir Ahmmad, Fumihiko Hirose,* Graduate School of Science and Engineering, Yamagata University, Japan

Nanometer-thick TiO_2-channel thin-film transistors (TFTs) are promising not only as high surface-sensitive sensors but also as active-matrix switching devices. InGaZnO (IGZO) has been used as a high-mobility TFT channels, offering around 10 cm^2/Vs. However, IGZO includes rare metals such as indium and gallium, leading to issues related to high cost geopolitical risks. On the other hand, TiO_2 is abundant on earth, non-toxic, although the field effect mobility of TiO_2-TFT was reported to be low due to defects in the film. In this study, the drain current enhanced TiO_2 TFTs were developed using atomic layer deposition.

We fabricated TiO_2-TFTs with a channel thickness of 16 nm as shown in Fig. 1, in which the channel surface was covered with an aluminum-silicate and SiO_2 periodical stacks. The stack layer serves as both the alkali metal absorber in the chloride solution and the meal diffusion source. The TiO_2 channel was deposited by atomic-layer deposition, followed by being annealed in dry air to induce crystallization. TFT samples were immersed in the alkali metal chloride solution, and it was assumed that the adsorbed metals were automatically diffused to the channel layer, which might contribute to deactivating the defects in the channel layer.

We confirmed the enhanced drain currents with CsCl and NaCl solutions as shown in Fig. 2. This suggests their potential as a high-mobility TFT. The effective mobility was calculated to be 83 and 46 cm^2/Vs for Cs and Na, respectively. XPS measurements suggested a reduction of TiO_2, which might contribute to the deactivation of the Oxygen-deficiency-related defects in the TiO_2 channel layer. In the conference, we shall discuss the current enhancement mechanism and applicability as an active-matrix switching devices.

AA-TuP-14 Exploring Dopant Candidates to Improve the Electrical Properties of TiO_2 Dielectric Thin Film, ***Seungwoo Lee***, *Gaeul Kim,* Kyung Hee University, Republic of Korea*; Hansol Oh, Hanbyul Kim, Donghun Shin, Yongjoo Park,* SK trichem, Republic of Korea*; Woojin Jeon,* Kyung Hee University, Republic of Korea

Dynamic random-access memory (DRAM) has been continuously scaled down to reduce production costs and increase integration density, thereby reducing the area occupied by cell capacitors and decreasing cell capacitance. This decrease in cell capacitance reduces sensing margin in read operations. Therefore, a material with a higher dielectric constant (*k*) is required as an insulator in DRAM capacitors to recover cell capacitance. TiO_2 in the rutile phase is an attractive candidate due to its high *k* value (>100) and compatibility with atomic layer deposition. However, it has leakage current issues due to its small bandgap (~3 eV). Therefore, suppressing leakage current via conduction band offset control between TiO_2 and the electrode film, such as Al doping, was effective. However, Al doping significantly decreases the capacitance density of TiO_2.

In this work, we evaluated the effectiveness of Mg, Sc, Gd, and In as alternative dopants for replacing Al. Crystallinity of each doped TiO_2, as a function of dopant and concentration, was analyzed by grazing-incidence X-ray diffraction, and the trend was consistent with dopant formation energy results obtained from density functional theory (DFT)-based simulations. Additionally, we evaluated the electrical properties of each doped TiO_2 and elucidated the dopant-dependent mechanism of electrical properties changes using X-ray photoelectron spectroscopy analysis and DFT simulations. Consequently, the Sc dopant did not significantly degrade the dielectric constant of TiO_2 among dopant candidates, thereby further improving the electrical properties by controlling the Sc doping concentration gradient.

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AA-TuP-15 Leakage suppression and memory window optimization via Gd-doped HfO_2 charge-trap layers in 3D NAND, ***Lee Jonghyeok***, *Jeon Woojin,* Kyung Hee University, Republic of Korea*; Nam Jihun,* Kyung Hee university, Republic of Korea*; Oh Hansol, Kim Hanbyul, Park Yongjoo,* SK trichem, Republic of Korea

Three-dimensional NAND (3D NAND) memories demand charge-trap stacks that provide wide memory windows at low programming voltages for reliable multi-level cell operation and reduced cell-to-cell interference. Hafnium oxide (HfO_2) has emerged as a promising charge-trap layer material because of its high dielectric constant and strong trapping capability.[1]However, uncontrolled intrinsic defects and non-uniform trap distributions in pristine HfO_2 often lead to leakage current and unstable charge storage.

To address these issues, previous studies have reported that Gd doping was employed to engineer the trap characteristics of HfO_2.[2]The substitution of Hf^{4+} by Gd^{3+} induces local lattice distortion and defect complexes, which suppress shallow oxygen-vacancy-related traps and generate energetically deeper trap states. These deep traps enhance charge confinement and suppress leakage pathways, resulting in an enlarged memory window and improved retention characteristics.

In this work, $Al_2O_3/HfO_2/Al_2O_3$ capacitors with Gd-doped HfO_2 layers (1–10%) were fabricated and evaluated using incremental step pulse programming. The 5% Gd-doped HfO_2 stack exhibited the widest memory window and the most efficient programming behavior, indicating an optimal deep trap density for charge storage. Electrical measurements further revealed that Gd doping improves the blocking characteristics by reducing leakage current, thereby enhancing charge retention performance.

Post-metallization annealing at 400 ℃ significantly modified the trap distribution, promoting the formation of deeper trap states and improving programming efficiency. In contrast, excessive Gd doping (≥10%) led to degraded hysteresis behavior, suggesting leakage-dominated transport due to excessive defect generation.

These results demonstrate that Gd-induced deep trap engineering, combined with thermal processing, provides an effective strategy for optimizing HfO_2-based charge-trap stacks, enabling low-voltage, wide-window, and high-reliability operation for future 3D NAND flash memory applications.

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AA-TuP-16 Leakage Current Suppression at Grain Boundary in Rutile TiO_2 via La Doping, ***Gaeul Kim***, *Seungwoo Lee,* Kyung Hee University, Korea (Democratic People's Republic of)*; Hansol Oh, Hanbyul Kim, Donghun Shin, Yongjoo Park,* SK Trichem Co., Ltd., Korea (Democratic People's Republic of)*; Woojin Jeon,* Kyung Hee University, Korea (Democratic People's Republic of)

As dynamic random-access memory (DRAM) devices continue to scale down, the reduction of equivalent oxide thickness in cell capacitors has become increasingly critical, necessitating the use of high-k dielectric materials. Rutile-phase TiO_2 is a representative high-k material with dielectric constant of approximately 100 or higher; however, its relatively narrow bandgap and donor levels associated with oxygen vacancies lead to high leakage current. Therefore, acceptor doping using trivalent cations, particularly Al, has been investigated as an approach to reducing leakage current.

In this study, we propose a new approach to effectively suppress leakage current through grain boundary in TiO_2. Grain boundary is defect-rich regions where electron accumulation can readily occur, thereby acting as leakage current conduction paths. To suppress leakage current through grain boundary, La was doped to induce segregation toward grain boundary. Because La^{3+} has a larger ionic radius than Ti^{4+}, its substitution into the TiO_2 lattice is limited, and this significant ionic radius mismatch can promote preferential segregation of La at grain boundary. After La doping, post-deposition annealing (PDA) was performed to induce La segregation. Grazing-incidence X-ray diffraction analysis revealed that the rutile TiO_2 peak shifted toward higher angles after PDA at 600 ℃ compared to the as-deposited state. This shift indicates a reduction in the d-spacing of TiO_2 as La initially present within the lattice migrated to grain boundaries during annealing, supporting the occurrence of La grain boundary segregation. Furthermore, electrical characterization showed a significant reduction in leakage current in La-doped TiO_2 dielectrics, which is attributed to the effective suppression of grain-boundary-related conduction paths. These results suggest a novel mechanism for reducing leakage current in rutile TiO_2-based high-k dielectrics and provide a promising approach for next-generation DRAM capacitor applications.

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AA-TuP-17 Development of Si-C-Si Bond-Containing Precursors for SiOC Thin Films, ***Kazutaka Takahashi***, *Akihiko Ohtsu, Tomonori Takahashi, Aina Ushiyama, Motomasa Takahashi, Shuhei Yamaguchi, Masaki Morita, Takeshi Yoshioka, Nobuhiko Takano, Hiroshi Komatsu,* FUJIFILM Corporation, Japan

This study reports on the development of novel organosilicon precursors specifically tailored for the atomic layer deposition (ALD) process of silicon oxicarbide (SiOC) thin films. First, to design precursor structures effective for ALD, we established a computational framework for systematically evaluating the adsorption energy, activation energy, and reaction energy of precursors. This enabled the selection of an optimal precursor structure with a stable Si-C-Si backbone. Subsequently, we successfully synthesized the precursor based on a unique chemical path. The resulting ALD of the precursor demonstrated obviously higher growth per cycle (GPC) compared to conventional precursors, and the ALD film included Si-C-Si bonds well. Furthermore, by analyzing dependency of process temperature, precursor dose time, and ozone dose time, ALD based film growth mechanism was clarified. A notable challenge in high–temperature ALD processes is that the carbon concentration in the film generally decreases as process temperature increases. Moreover, process modifications aimed at increasing the carbon ratio typically led to a deterioration in both GPC and in–plane uniformity. In this work, however, by carefully optimizing the process conditions, we successfully achieved high carbon concentration, high GPC, and good in–plane uniformity simultaneously, even under high–temperature deposition conditions.

AA-TuP-18 Modeling of Negative Capacitance FETs for Sub-60 mV/dec Switching through PEALD-HZO Ferroelectric Thin Films, ***Bohyun Kim***, *So Won Kim, Jae Hyuk Choi, Hee Chul Lee,* Department of Advanced Materials Engineering, Tech University of Korea

Since the discovery of negative capacitance (NC) in ferroelectrics, extensive research has been conducted in the field, with the Negative Capacitance Field-Effect Transistor (NC-FET) emerging as a breakthrough technology. NC-FETs have attracted significant attention for their ability to lower the subthreshold swing (SS) below the fundamental limit of 60 mV/dec at room temperature, making them highly advantageous for suppressing leakage current and realizing ultra-low-power devices.

In our previous study [1], we successfully deposited (HZO) ferroelectric thin films with relatively good polarization and reliability characteristics using a Co-Plasma ALD (CP-ALD) process, which simultaneously utilizes both direct and remote plasmas, as shown in Fig. 1. However, the inherent polarization hysteresis of ferroelectrics remains a significant challenge for switching device applications. To precisely control the NC characteristics, optimized capacitance matching through a ferroelectric-dielectric (FE/DE) stacked structure is essential [2].

Based on the characteristics of the HZO thin films deposited via our group's CP-ALD process, we modeled the electrical performance of MFIS-structured NC-FETs by stacking ferroelectric and dielectric layers, as illustrated in Fig. 2(a). For a 15-nm-thick ferroelectric HZO layer, the subthreshold swing (SS) was modeled as a function of the dielectric layer thickness, using Al_2O_3(k9) and HfO_2(k25) as the dielectric materials.

The results indicate that sub-60 mV/dec SS values are achieved when the dielectric thickness is below 1.4 nm for Al_2O_3 and 5.4 nm HfO_2. In particular, the most stable and lowest SS values were observed at thicknesses of 1.4 nm for Al_2O_3 and 3.8 nm for HfO_2. Especially, HfO_2 exhibited a much broader thickness window for maintaining an SS below 60 mV/dec compared to Al_2O_3. The optimized SS of the NC-FET improved by up to 12 mV/dec compared to that of a conventional MOSFET without a ferroelectric layer.

Additionally, to analyze the NC phenomenon in a practical polarization-switching environment, we will present modeling results based on the Nucleation-Limited Switching (NLS) theory, which accounts for the time-dependent transient polarization characteristics of ferroelectrics.

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AA-TuP-19 Co-reactant-Assisted Thermal ALD of TaN Using a High-Thermal-Stability Liquid Ta Precursor for Advanced DRAM Capacitors, ***Yejin Han***, Kyung Hee University, Republic of Korea*; Hyunju Jung, Hanbin Lee, Shinbeom Kim,* EGTM Co., Ltd., Republic of Korea*; Jiyeon Han,* EGTM Co.,, Ltd., Republic of Korea*; Woojin Jeon,* Kyung Hee University, Republic of Korea

As dynamic random-access memory (DRAM) continues to scale down, electrode materials with high work functions are required to suppress leakage current and maintain sufficient capacitor performance.[1] TiN has been widely used as a conventional DRAM capacitor electrode material; however, alternative electrode materials with higher work functions are increasingly required for next-generation DRAM capacitors.[1] Among various candidates, TaN has attracted considerable attention owing to its high work function, excellent thermal stability, and diffusion barrier properties.[2] However, TaN deposition is commonly performed using plasma-enhanced atomic layer deposition, which suffers from plasma-induced damage and limited conformality in high-aspect-ratio structures. Although thermal atomic layer deposition (ALD) provides superior conformality, insufficient nitridation and incomplete ligand removal often degrade film quality.In this work, a co-reactant-assisted thermal ALD process was developed using a newly developed high-thermal-stability liquid Ta precursor, EGTM Ta, and NH3 reactant. To enhance nitridation and facilitate ligand removal, tert-butyl iodide (TBI) was introduced between the precursor and NH3 exposure steps. X-ray photoelectron spectroscopy analysis using the conventional Ta precursor TBTEMT confirmed that TBI incorporation increased the TaN fraction, indicating enhanced nitridation during thermal ALD. In addition, reduced film resistivity was observed after TBI incorporation, demonstrating improved film quality through impurity reduction. Owing to its superior thermal stability, EGTM Ta enabled thermal ALD at elevated temperatures and further enhanced the effectiveness of the TBI co-reactant, resulting in improved TaN formation and electrical properties.These results demonstrate that the combination of an iodine-based co-reactant and a high-thermal-stability liquid Ta precursor is an effective strategy for high-temperature thermal ALD of TaN. The proposed process enhances nitridation, suppresses impurity incorporation, and improves film quality while maintaining the conformality advantages of thermal ALD, providing a promising route for next-generation DRAM capacitor electrode applications.**References** [1] W. Jeon, J. Mater. Res. 35, 7 (2020). [2] P. Patsalas et al., Mater. Sci. Eng. R Rep. 123, 1 (2018).

AA-TuP-20 Minimisation of Platinum Loading on the Porous Transport Layer in Pem Water Electrolysers, ***Athina Tzavara-Roussi,*** *Volkert van Steijn, Ruud van Ommen,* Delft University of Technology, Netherlands

Proton exchange membrane water electrolysis (PEMWE) is considered a highly promising technology for converting intermittent renewable electricity into green hydrogen, yet it relies on scarce platinum-group metal for their catalytic activity and chemical stability, which could significantly limit scalability. The porous transport layer (PTL) is a critical component, typically made of titanium, on the anode of PEM electrolysers, since it facilitates the electron and mass transfer between the catalyst sites and the bipolar plates. A major challenge stems from the oxidation of the PTL in the highly oxidative anodic environment, which significantly reduces electrical conductivity and limits catalyst utilization. To protect the contact points between the anodic layers, the commercial solution involves the platinization of the PTL. However, this approach not only increases further the manufacturing costs, but also results in poor coating conformity thus risking its long-term durability.

This study investigates the use of ALD to achieve a conformal and uniform Pt coating on the PTL surface, in combination with evaporation to increase the coating thickness. We examine how the Pt loading, morphology, and thickness affect the performance and durability of the layer in a 4 cm^2 single PEM cell, identifying which coating configuration provides optimal protection for the PTL. Finally, we evaluate the deposition of iridium oxide to transform the PTL into a porous transport electrode and assess its electrochemical performance.

This project receives a Dutch National Growth Fund contribution from the programme NXTGEN HIGHTECH.

AA-TuP-21 Characterization of ALD-like SiCO Layers for MOL and BEOL Applications: Influence of Etching Plasma and Wet Clean, ***Alexandre Ponchon***, *Emmanuel Petitprez, Pierre Brianceau, Benoit Martin, Melanie Dartois, Antoine Raison, Nicolas Gauthier,* CEA/LETI-University Grenoble Alpes, France

Atomic Layer Deposition (ALD) enables precise control of layer thickness at the atomic level, making it more suitable than Chemical Vapor Deposition (CVD) for etch stop layers (ESLs) in advanced transistor manufacturing. ESLs are crucial for precise pattern transfer and underlying structures protection during etching. As device dimensions continue to scale, there is an increasing demand for ultrathin and uniform ESLs with well-controlled thickness and etch selectivity.

In this work, we investigate the use of SiCO layers deposited by Single Precursor Activated Radicals Chemistry [1] (SPARC) process (a new technique in-between CVD and ALD), as SiN dry etch stop layer for MOL (middle of line) and BEOL (back-end of line) applications. We focus on the impact of the carbon elemental composition on the SiCO layer's resistance to standard wet clean chemistries and its ability to maintain ESL properties under etching plasma exposure.

We use 30nm thick SiCO layers, deposited at 400°C, with carbon content varying from 3% to 13%. We characterize the material resistance to standard wet clean chemistries and to two plasma etching chemistries (CH3F/O2/Ar and CH3F/H2), by monitoring the layer thickness before and after the process steps using a spectrometric ellipsometer. We assess the impact of the etching plasma on the remaining SiCO material through Secondary Ion Mass Spectrometry (SIMS) elemental depth profiles.

Results show that SiCO layers exhibit high resistance to wet clean chemistries, with minimal thickness loss observed only in low carbon content films exposed to diluted HF, and its resistance increases as the carbon composition increases. After exposure to the plasma chemistries used for SiN dry etch, all SiCO layers show thickness reduction, with oxygen-based plasma causing greater removal than hydrogen-based plasma. Plasma etching modifies a few nanometers of the remaining SiCO film, which becomes an O-rich layer that can be removed with a dHF dip. The altered layer thickness is more substantial with hydrogen-based plasma, and higher carbon content results in shallower modifications.

These findings show that this SiCO layer deposited by SPARC is a promising material for MOL and BEOL ESL applications as it has a high resistance to both dry and wet etching processes while being easily removable after undergoing a plasma etch.

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AA-TuP-22 In Situ, Simultaneous Spectroscopic Ellipsometry and Quadrupole Mass Spectrometry Studies of Aluminum Doped ZnO Etching Using β-Diketones, *Maahir Rahi,* ***Terrick Mcnealy-James***, *Justin Moore, Titel Jurca, Parag Banerjee,* University of Central Florida

Atomic layer etching (ALE) offers sub-nm level control over film removal and presents promising solutions to address patterning challenges in device manufacturing. These mechanisms become particularly important when the extended atomic structure of films such as crystal facets, grain boundaries, and dopants are taken into consideration.

In this work, we investigate the thermal ALE of aluminum doped zinc oxide (Al:ZnO) using β-diketonate-etchants such as, acetylacetonate (Hacac) and hexafluoro acetylacetonate (HFacac), by depositing monolayers of Aluminum into Zinc oxide. We utilize *in situ* spectroscopic ellipsometry (SE) and quadrupole mass spectrometry (QMS), enabling real time correlation between thickness evolution and reaction by-products. By coupling these techniques, this work provides insight into kinetics, reaction pathways, and the role of dopants.

AA-TuP-23 Terpineol Doped ALD Al_2O_3 Films for Low-K Materials: Effect of Terpineol Ratio and Metal Precursor Size on Structural and Dielectric Properties, ***Sovendo Talapatra**, Noah Zahn, Nicholas Strandwitz,* Lehigh University

Research on low-κ dielectric materials is becoming critically important to deal with capacitance delays of due to decreasing dimensions of integrated circuits. Herein, we will report the structural and dielectric properties of terpineol-doped Al_2O_3 films where terpineol acts as a sacrificial agent or porogen, leaving porosity in the films after post-deposition annealing treatment. Terpineol-doped films were deposited by atomic layer deposition (ALD) and the modification of the porosity by changing the ratio of terpineol pulse in between the metal precursor and H_2O co-reactant was explored. The choice of metal precursor also influences the porosity generation in the film because of the steric hindrance and reactivity of the precursor. Three metal precursors, trimethylaluminum (TMA), aluminum tri-sec-butoxide, and tri-i-butylaluminum will be used to study the density, dielectric constant of the films. X-ray reflectivity will be used to measure the density of the films. For TMA to terpineol ratio 1:1, initial result showed 17% decrease of density for as deposited terpineol doped films than ALD Al_2O_3 at 120ºC. Dielectric constant of the films will be measured using capacitance-voltage measurement. For as-grown terpineol-doped films the initial measurement also showed dielectric constants as low as 4 compared to a value of ~7 for ALD grown Al_2O_3. Our work shows that small molecule inclusions in ALD is a useful strategy for the growth of porous and low-κ thin films, while still retaining the benefits of precise thickness control and conformality afforded by ALD.

AA-TuP-24 Dielectric Nitride Using Fast Remote Plasma ALD for Power Devices, ***Arpita Saha**, Elliot Gay, Dmytro Besprozvannyy, Michael Powell, Tania Hemakumara, Aileen O'Mahony,* Oxford Instruments Plasma Technology, UK

Gallium Nitride (GaN) has recently expanded into power electronics, RF,microLEDs and VCSELsmarkets.The adoption of GaN transistors in high volume consumer-based power electronicsis driven by the need for smaller, faster, efficient mobile device chargers.It has been predicted the GaN power device market will reach $3B by 2030[1]supported by a broader range of applications including renewable energy, data centres, electric vehicles, and infrastructure for 5G and 6G networks.

These emerging GaNmarkets require uniform,conformal,low damage plasma processing solutions optimised for 200 mm wafers to improve device performance,throughput, andyieldat reduced cost.Plasma enhanced atomic layer deposition (PEALD) has been used in GaN transistors for low damage,[2]uniform passivation layers (Al_2O_3,[3] SiN), as a method of optimizing the interface using native oxide removal nitridation[4,5]followed by deposition of high-quality nitrides like AlN.

High throughput plasma ALD of SiN is beneficial for GaN device processing at low temperature (≤500 °C) compared to LPCVD (≥700 °C)and thermal ALD (>450 °C) without compromising on conformality (compared to PECVD)[10]or uniformity up to 200 mm wafer size. PEALD SiN has also been shown to reduce trap defect density in GaN transistors compared to other deposition techniques and materials.[11]Optimisation of the plasma processing parameter scan achieve SiN films with tuneable growth rate,composition,and refractive index.[12, 13].

PEALD processes forAlN and SiN have been developed achieving excellent thickness and refractive index uniformity across 200 mmSi wafers using Oxford Instruments Atomfab ALD system which uses apatented capacitively coupled (CCP)[3] remote plasma source. Using Oxford Instruments' novel CCP remote plasma source, and a low chamber volume, increase in deposition rate has been achieved when comparing to an inductively coupled plasma source (ICP) process. For example, we have been able to achieve 8 times faster deposition rate for AlN films using our CCP remote plasma source compared to ICP plasma.The composition of the AlN and SiN films were measured by XPS resulting in low C% and O% content. The ToF-ERDA showed low H% content in SiNx films while the wet-etch rate was better for the films produced using the CCP plasma source compared to the films produced by ICP plasma source. The breakdown voltage and the dielectric constant for the as deposited SiNx film obtained was >10.5 MV/cm and >6 for 30 nm film respectively.

To support the production ramp of the GaN transistors, high throughput tuneable AlN and SiN processes using plasma ALD along with optimized surface pre-treatment has been developed by Oxford Instruments negating the need for extended plasma exposure,high temperature depositionor temperature ramping within the process.The estimative wafers produced per hour for AlN (3 nm films) is 11 WPH and for SiNx (5 nm films) is 10 WPH.

AA-TuP-26 Impact of Oxidant on Conformal HZO ALD in High Aspect Ratio Structures, ***Soham Shirodkar**, Dushyant Narayan,* The University of Texas at Dallas*; Dan N. Le,* RASIRC, University of Texas at Dallas*; Thi Thu Huong Chu, Soubhik De, Minjong Lee,* The University of Texas at Dallas*; Adrian Alvarez, Lorenzo Diaz,* RASIRC*; Jiyoung Kim,* The University of Texas at Dallas

The scaling of advanced DRAM technologies requires complex structures with high aspect ratio (HAR) trenches and cavities and is currently transitioning to 3D integration to sustain performance improvements.[1] Hafnium based oxides are key materials for the cell capacitor in DRAM cells due to their high dielectric constant and wide bandgap. To achieve conformal growth in HAR structures, ALD processes often use large precursor and oxidant doses to ensure reactant transport into deep features [2]. However, excessive oxidant dosing can promote undesirable interfacial oxidation, particularly on metal electrodes. To address this, we identify differences in oxidant efficiency during HAR filling and evaluate the role of various counter-reactants on conformal growth.

To understand the effect of counter reactant choice, we first investigated growth characteristics on planar substrates. We found that the oxidant dose required to reach saturation was different for each oxidant. Namely, we found that H_2O_2 required a smaller dose than O_3 to saturate each ALD cycle. Saturation at a reduced oxidant dose implies a potential for improved filling in HAR structures at lower doses while mitigating excessive interfacial oxidation due to high dosing.

Based on the observations for planar substrates, vertical HAR substrates with AR ranging from ~20:1 up to ~60:1 were used to evaluate the conformality of each process. Furthermore, to enable quantification of penetration depth, specially designed horizontal Ultra-HAR structures with AR up to 10,000:1 were used, and analysis of growth areas were performed using SEM and EDX (Fig. 1). The extent of growth into the cavity was used to assess the deepest achievable filling as a function of both oxidant and precursor dosing. Alongside the horizontal structures, conformality was also evaluated in vertical trenches with smaller critical dimensions, providing access to more extreme confinement where precursor transport is further limited (Fig. 2). We found that increasing precursor dose improves transport into confined geometries, with signatures of oxidant-dependent effects on HAR filling. Overall, these results show that oxidant choice plays an important role in ALD growth in HAR structures for the stringent demands of next-gen semiconductor devices.

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AA-TuP-27 Stable High-k Morphotropic Phase of $HfZrO_4$ Using Uniformly Distributed Dopants, ***Nguyen Vu**, Charlene Chen, Sunil Ghimire, Ray Meck, Jared McWilliams,* EMD Electronics, USA

Since the 1950s, the morphotropic phase boundary (MPB) has attracted considerable attention due to the anomalous increase in the dielectric constant in this region. It is now gaining rapid growth in research on hafnia-based dielectrics as a novel approach to achieve low equivalent oxide thickness (EOT) without sacrificing leakage. Unlike the traditional nanolaminate approach, this work investigates the formation of the MPB phase in HZO dielectrics with uniformly distributed dopants through atomic layer deposition and annealing within the back-end-of-line thermal budget. It is found that the more homogeneous the dopant distribution, the better the dielectric performance. The resulting doped HZO with a physical thickness of 50 Å exhibits a low leakage current of $2x10^{-5}$ A/cm^2 and an EOT of 5.4 Å. Different strategies for achieving the desired dopant distributions are discussed, highlighting the potential of precursor development to reach the optimal performance.

AA-TuP-28 ALD Oxide Coatings for Anti-Stiction MEMS Applications Compatible with 500 and 1000 °C Wafer Bonding, ***Eric Reed**, Matthew Weimer, Arrelaine Dameron,* Forge Nano*; Robert MacDonald, David Lin,* GE Aviation, USA*; Mohammad Megdadi,* University of Nebraska - Lincoln*; Mary Ann Maher,* Soft MEMS

As MEMS devices continue to shrink and the operational range demands increase, they increasingly suffer from irreversible stiction, in which surface forces, such as van der Wall forces and electrostatic forces, exceed the forces required to separate moving components, the restoring force. Some

attempts to reduce surface adhesion include the reduction of surface energy by application of self-assembled monolayers (SAM) or diamond-like carbon coatings (DLC) and low surface area contact points, such as bump stops. However, these methods become less effective as MEMS devices continue to approach nanoscales. For example, SAM coatings become more susceptible to defects and non-conformal films as the aspect ratio increases. Additionally, DLC and SAM coatings are incompatible with high-fidelity packaging methods, like direct wafer bonding, which occurs under >1000 °C annealing conditions. DLCs suffer from adhesion instability while SAM coatings completely degrade at this temperature. Atomic Layer Deposition (ALD) overcomes these deficiencies by providing conformal, temperature-stable films. Engineering surface roughness and film stability is, therefore, one path to improving device reliability. This study investigates which ALD thin films provide the greatest surface roughness with sufficient adhesion to silicon substrates. Silica (SiO2), hafnia (HfO2), and titania (TiO2) films were deposited on Si ⟨100⟩ coupons using thermal ALD and subsequently annealed in an inert environment, at 500 °C and 1000 °C, to simulate various MEMS wafer bonding processes. The films were evaluated for changes in crystallinity, surface roughness, and composition. SiO2, used as a control, exhibited minimal changes in structure and roughness. HfO2, initially polycrystalline, showed increased crystallinity and surface roughness with annealing while maintaining film stability. When applied to a MEMS test structure, the 1000 °C annealed HfO2 film showed a significant reduction in stiction, compared to the coated features. In contrast, TiO2 underwent a significant crystallographic phase transition at >700 °C and delaminated, likely due to film stress. These results indicate that polycrystalline HfO2 offers a stable, roughened surface capable of reducing attractive forces responsible for MEMS stiction failures. Future work will evaluate thermally deposited ALD HfO2 directly on MEMS accelerometers and gyroscopes to quantify its impact on device performance and reliability.

AA-TuP-29 Enhancing ZrO_2–based DRAM capacitor performance by employing atomic layer deposited In_2O_3 electrode via Mo doping, ***Hunseok Son****, Woojin Jeon,* Kyung Hee University, Republic of Korea

As dynamic random-access memory (DRAM) scales down to achieve higher integration, electrode engineering to mitigate insufficient capacitance and excessive leakage current remains a critical challenge. TiN electrodes and ZrO_2 dielectrics are widely used in metal-insulator-metal (MIM) capacitors because of their excellent process compatibility. However, TiN electrodes deplete oxygen from ZrO_2 at the ZrO_2/TiN interface via an oxygen-scavenging effect, forming undesirable TiO_xN_y. This accelerates leakage and degrades performance.[1] The formation of these oxygen defects degrades not only the electrical characteristics but also the overall performance of the MIM capacitor. The initial spacing is not correctly formatted. Furthermore, nitrogen diffusion into ZrO_2 reduces the bandgap, resulting in degradation of leakage current characteristics.[2] Therefore, oxide-based electrodes are more suitable for use with ZrO_2 than nitrogen-based electrodes. To overcome these limitations, we propose an approach that uses Mo-doped In_2O_3 bottom electrode grown by atomic layer deposition (ALD). During thermal treatment, Mo-doped In_2O_3 exhibits a change in oxidation state to Mo^{4+}, which substitutes for In^{3+}, resulting in high electrical conductivity due to increased free electrons and low resistivity. [3] Furthermore, its low roughness provides excellent electrode characteristics for MIM capacitors. [4] In terms of crystallinity, here to, the initial spacing is incorrect. The cubic phase In_2O_3 (400), formed by Mo doping in In_2O_3, exhibits good crystallographic compatibility with the tetragonal phase ZrO_2 (002). The formation of t-ZrO_2 (002) enables higher capacitance in ZrO_2-based MIM capacitors fabricated on Mo-doped In_2O_3. The high work function (~5 eV[5]) of Mo-doped In_2O_3 provides a distinct advantage over TiN (~4.2 eV[6]). This high work function contributes to leakage suppression, thereby enhancing the device's overall performance. Additionally, In_2O_3 has a significantly lower oxygen vacancy formation energy (~2.4 eV) than ZrO_2(~6.2 eV), enabling oxygen transfer to ZrO_2.[5] This mechanism not only suppresses the formation of sub-interface oxides, unlike TiN electrodes, but also reduces defect density within the ZrO_2 layer, minimizing unwanted conduction and improving interface stability. Consequently, replacing TiN with the ALD-grown Mo-doped In_2O_3 bottom electrode offers a practical, scalable solution. Mo-doped In_2O_3 provides sufficient capacitance while suppressing leakage current and enhancing stability, thereby strengthening the integrity of the MIM capacitor structure. This paves the way for continued dielectric scaling and improved reliability in advanced DRAM technology.

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AA-TuP-30 Advanced Seamless Lateral Gap-fill Process for 3D Structures via a New Approach, ***Yudeuk Kim****, Seunghee Cho, Kwangseon Jin,* Wonik IPS, Republic of Korea*; Hoon Kim,* Wonik IPS*; Wontae Noh, Taewan Lee, KYUNGPIL NA, Jaehun Lee, Jiwon Moon, Hyung mook Lim,* Wonik IPS, Republic of Korea

Like 3D NAND scaling progresses, the integration of 3D DRAM and advanced logic architectures requires highly conformal dielectric gap–fill capability within increasingly complex high–aspect–ratio structures. Conventional deposition schemes optimized for vertical profiles exhibit insufficient step coverage in lateral cavities, resulting in seam and void formation due to precursor transport limitations and restricted surface reaction accessibility. Moreover, the enlarged effective surface area significantly reduces throughput, forcing reliance on iterative deposition–etchback cycles that remain inefficient and inherently unsuitable for uniform lateral gap–fill.

To overcome these limitations, a novel ALD based gapfill strategy has been developed, enabling fully seamless void free filling across both vertical and lateral geometries. TEM analysis confirms that while conventional processes show pronounced internal seams shown in Fig. 1 (a), the newly engineered process demonstrates complete elimination of interfacial defects, ensuring structurally dense and continuous films throughout the entire 3D topology in Fig. 1 (b). This approach delivers improved structural robustness, enhanced conformality, and high productivity, positioning it as a key enabling technology for next generation high density 3D device fabrication.

AA-TuP-31 ***Modeling the Dynamics of Surface Coverage in Atomic Layer Deposition for Multilayer Lateral Trench Structures*****, *Jin Hak Kim****, Yoon Jae Won, Jun Soo Shin,* WONIK IPS, Republic of Korea

As AI technology advances and the need for high-performance memory semiconductors increases, 3D DRAM manufacturing technology is one of the promising technology to increase memory capacity. To reduce high experimental costs and increase process development speed, it is important to estimate processing time in the atomic layer deposition process. As the number of lateral trenches increases, the adsorption area increases compared to when there are only vertical trenches. Our simulation shows that the minimum saturation time for conformal atomic layer deposition is proportional to the aspect ratio in the lateral and vertical directions. Due to the effect of gas particles being re-emitted from the bottom of the trench, the minimum surface coverage area is located away from the bottom of the lateral and vertical trench surfaces. The result is similar to those in a paper simulating adsorption inside lateral channels.1

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AA-TuP-32 Nucleation Dependence of ALD on Diamond for Surface Processing in Quantum Applications, ***Jessica Jones****, Jeffrey Elam,* Argonne National Laboratory, USA

The surface termination and interfacial interactions of materials for quantum technologies are critical.Use of atomic layer deposition (ALD) has been explored to provide insight on the chemical environment of the surface while passivating the surface.We explore the nucleation and growth of ALD Al_2O_3 and TiO_2 on diamond surfaces used for quantum sensing.We demonstrate the suppression of dark spins on diamond surface after coalescence of the TiO_2 ALD film on the surface.Additionally, we demonstrate that the nucleation of ALD Al_2O_3 using dimethylaluminum isopropoxide (DMAI) and water is sensitive enough to distinguish between the common surface termination types (H- terminated and O-terminated).We also evaluated methods to pretreat the diamond surface prior to passivating the surface with ALD Al_2O_3. We used in situ spectroscopic ellipsometry measurements to monitor the surface reactions and evaluate the ALD Al_2O_3 nucleation process as a function of different ex situ and in situ surface pretreatments. We found that in situ water dosing and high vacuum annealing provided the most favorable environments for nucleation of ALD Al_2O_3 using DMAI and water ALD. Hydrogen termination passivated both smooth and rough surfaces while triacid cleaning passivated the smooth surface only, with striking effectiveness.

AA-TuP-33 Atomic Layer Deposition on Reduced Activation Ferritic Martensitic Steel for Nuclear Fusion Applications, ***Soren Bentley***, UK Atomic Energy Authority, UK; *Zachary Robinson, Mark Wittman,* University of Rochester; *Matthew Sharpe,* University of Rochester, UK; *Rashad Ahmadov, Josh Ruby,* University of Rochester; *Jeffrey Woodward,* Naval Research Laboratory; *Alexander Kozen,* University of Vermont

Nuclear fusion holds immense potential to reshape the global energy landscape. To develop mature technologies that can be deployed at power-plant scale, numerous materials-science challenges must be solved. One critical example is the safe, efficient, and loss-free handling of tritium (hydrogen-3), an essential fuel for fusion energy. Tritium permeates many of the materials used in reactor components, leading to structural embrittlement and other hazards associated with the fuel's radioactive properties. Atomic layer deposition (ALD) is emerging as a promising technique for the development of Al_2O_3 permeation barrier coatings that reduce loss of tritium. ALD's ability to produce high-quality, uniform films across complex geometries and components makes it advantageous compared to techniques limited to planar substrates. Though ALD Al_2O_3 coatings are well studied on semiconductor-relevant substrates, the work presented here reports the use of a custom-built ALD system to carry out the first syntheses on fusion-grade reduced-activation-ferritic-martensitic (RAFM) steel.

Prior to deposition, 1 cm × 1 cm RAFM steel substrates were prepared by polishing them to ~15 nm root mean square surface roughness. Al_2O_3 films were then deposited using a thermal ALD process with trimethylaluminum (TMA) and water precursors. Deposition was performed at temperatures between 100–200 °C to determine optimal growth conditions. Once this was achieved, growth rate curves were measured.

The films were characterized using X-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD), X-ray reflectivity (XRR), and spectroscopic ellipsometry. Our XPS results indicate that the RAFM surface is predominantly iron, in addition to small quantities of chromium oxide. ALD films were primarily stoichiometric Al_2O_3, with some growth conditions resulting in a small aluminum hydroxide component. The XRR and ellipsometry data were used to determine film characteristics such as morphology and ALD film thickness. This required the development of a model in which the film was represented as three layers: a low-density surface oxide, a denser bulk oxide, and an interface oxide in contact with the substrate surface. Growth rate curves and other process development will be presented.

AA-TuP-36 ALD and Surface Chemistry of p-type Tin Oxides, *Asare Dua, Michael Foody,* Illinois Institute of Technology; *Bo Liu,* ***Adam Hock***, illinois Institute of Technology

Low temperature ALD of p-type conducting oxides remains a challenge, particularly as surface chemistry can dominate contact quality and therefore device performance as a function of overall scaling.Furthermore, the surface of p-type oxides is often susceptible to reaction with atmospheric oxygen and water, altering dopant concentrations and affecting process conditions.We have developed a new tin ALD precursor and utilized it for low-temperature, thermal ALD of p-type tin oxides.We have characterized the chemical and physical properties of the precursor, its ALD growth window, and resulting p-type film mobilities.We also have studied the effects of surface treatments on mobility and stability of the resulting films.

In this talk we discuss the results of these studies on p-type tin oxide thin films grown using a novel precursor.This includes QCM measurements under ALD conditions, solution model reactions, and synchrotron studies conducted at the Advanced Photon Source (APS) located at Argonne National Laboratory.The surface reactions of Sn precursors and half-reactions provide insight into the surface of the film and overall manufacturability of p-type oxides in the future.The results of these studies were applied to improved p-type oxide ALD, including doping strategies.Device characterization will also be discussed as time allows.

AA-TuP-37 Plasma-Enhanced Atomic Layer Deposition of Highly Conductive Cobalt Thin Films for Copper Alternative Interconnects, ***Hyeonbin Kim***, *Soo-Hyun Kim, Yeseul Son, Debananda Mohapatra,* Ulsan National Institute of Science and Technology, Republic of Korea

As semiconductor devices continue to scale down, conventional Cu interconnects face increased resistivity due to size effects and degraded reliability caused by electromigration. To overcome these limitations, alternative interconnect materials have been actively explored. Among them, cobalt (Co) has attracted considerable attention as a promising interconnect material owing to its high melting point (1768 °C), short electron mean free path (~7.8 nm), and excellent chemical stability. In this study, Co thin films were deposited by plasma-enhanced atomic layer deposition (PEALD) using a liquid Co precursor, bis(1,4-di-isopropyl-1,4-diazabutadiene)cobalt [$Co(dpdab)_2$]. Plasma reactants, including H_2, N_2, NH_3, and N_2+H_2 mixtures with H_2/N_2 ratios of 1, 3, 5, and 7, were employed, and depositions were carried out on thermally grown SiO_2/Si substrates at temperatures between 250 and 300 °C. The influences of reactant types, plasma power, and precursor and reactant pulse durations on the electrical resistivity of the Co thin films were systematically investigated. By optimizing the Co PEALD process parameters and applying post-annealing, impurity incorporation was effectively suppressed, thereby improving electrical performance. The structural, compositional, and morphological properties of the deposited Co thin films were analyzed by XRD, SEM, XPS, and TEM. As a result, high-quality Co thin films with a low resistivity of 17.4 μΩ·cm were obtained. Furthermore, the thickness-dependent resistivity behavior of the Co thin films was evaluated and compared with reported values for other alternative interconnect materials. Finally, the PEALD-grown Co thin films deposited under optimized conditions were applied as alternative Cu interconnects, and the detailed results will be presented at the conference.

Acknowledgments

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AA-TuP-38 Study of Void Suppressed TiN thin films deposited by ALD, ***Dong-Hoon Han***, *Jiwhan Kim, Moonkeun Kim, Suncheul Kim, Joonho Lee,* Samsung Electronics Co., Republic of Korea

Dynamic Random Access Memory (DRAM) continues to scale down, increasing the need to acquire low resistance and reliability for the cell transistor's word line and gate materials. Titanium nitride (TiN) offers advantages such as low resistance in confined spaces and high thermal stability, and therefore has been employed as the word line material for recent DRAM product. To achieve the required word line resistance after TiN deposition, a rapid thermal annealing (RTA) step is used to enlarge the TiN grain size. However, this process can generate voids within the TiN layer; these voids tend to form near the gate oxide, causing non uniform or elevated gate threshold voltage (Vth) and degrading transistor control performance. In this study, we developed a highly nucleated deposition method that suppresses void formation. When applied to the recent DRAM product, the void portion decreased from 8.8 % to 7.3 %, the production yield increased, and the tRDL (last data into row pre charge time) fail bit count dropped significant amount over 50%. The paper discusses two approaches for improving nucleation in atomic layer deposition (ALD): (1) reducing impurities and (2) enhancing surface reactions. These strategies are expected to deepen the understanding of surface engineering for ALD in next generation DRAM.

AA-TuP-39 Implementation of Vertical Selector-only Memory via ALD-grown GeXSeYTeZ Thin Films, ***Hyun Wook Kim***, *Ju Hwan Park, Se Hwan Jeon, Yoon Jae Hong, Dong Hyun Kim, Byung Joon Choi,* Seoul National University of Science and Technology, Republic of Korea

The development of next-generation non-volatile memory technologies is crucial to address the increasing demand for high-density storage and low power consumption.Selector-only memory (SOM) has emerged as a promising candidate due to its capability to integrate the selector and memory cell into a single device, enabling high-density stacking. In addition, it provides a potential pathway to address the fundamental data bottleneck limitations of the von Neumann architecture.In SOM, non-volatile '0' and '1' states are defined by two threshold voltages (Vth) under opposite polarities, and their difference, the memory window (MW), represents the device performance[1].

Se–Te-based multicomponent systems, such as GexSeyTez, have been widely reported to exhibit excellent threshold switching (TS) characteristics, high endurance (>10^{12} cycles), and a wide MW over a range of compositions[1,2].Despite these promising properties, most studies have been limited to physical vapor depositionprocesses, which suffer from poor conformality and are therefore unsuitable for high-aspect-ratio vertical architectures required for high-density integration.Atomic layer deposition (ALD) offers a viable solution due to its excellent conformality; however, its application to chalcogenide materials remains challenging due to complex

surface reactions, low precursor reactivity, and difficulties in achieving precise control of multicomponent compositions.

In this study, we developed an ALD process for ternary $Ge_xSe_yTe_z$ thin films to enable SOM operation in vertical structures. Germanium(II)-guanidinate,bis-trimethylsylil selenium, and bis-trimethylsylil tellurium precursors were used to enhance thermal stability and reactivity, and NH_3 gas co-injection was applied to optimize growth. The film composition was controlled by tuning the deposition temperature.The deposited films were analyzed in terms of impurity content, surface roughness, chemical bonding states, and surface morphology.Electrical properties were subsequently evaluated in both planar and vertical device structures, confirming stable TS behavior and reliable SOM operation.In planar devices, distinct MWs were observed depending on the growth temperature, with $Ge_5Se_3Te_2$ exhibiting a MW exceeding 0.7 V. In a vertical SOM device employing a double-stacked W/SiO_2 structure, a MW of approximately 0.4 V per layer was achieved, showing a trend consistent with that of the planar devices.

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AA-TuP-40 ALD-Grown Nickel Oxide Interlayer for Enhanced Performance of PbS Quantum Dot Photodetectors*, Zhenghao Xu, Junweichen Ge, Xuetong Zhou, Xinhong Cheng,* ***Li Zheng****,* Chinese Academy of Sciences, China

PbS colloidal quantum dot (CQDs) photodetectors (PDs) integrated with silicon offer a promising route toward low-cost, flexible infrared photodetection by combining solution processability with industrial scalability. However, their performance is fundamentally constrained by interfacial trap states and a significant band offset at the Si/CQDs interface, which act as non-radiative recombination centers and severely impede efficient carrier extraction, thereby limiting photoresponsivity. Here, we employ atomic layer deposition (ALD) as a precision interfacial engineering strategy and demonstrate the fabrication of high-quality nickel oxide (NiO) thin films at 200℃ using bis(N, N'-di-t-butylacetamidinato)nickel(II) (Ni-AMD) and water as precursors. By inserting an ultrathin NiO interlayer via ALD between the Si substrate and the PbS CQDs active layer, we achieve atomic-scale passivation of interfacial traps, optimized band alignment, and enhanced carrier transport efficiency.

Atomic force microscopy (AFM) and scanning electron microscopy (SEM) reveal that the ALD-grown NiO film exhibits superior compactness, markedly reduced porosity, and a surface roughness below 0.5 nm, attributed to the optimized pulse time (1 s) and prolonged purging process (15 s) for the Ni precursor. The resulting devices show a dark current density suppressed by ~80% and a responsivity exceeding 500 mA/W, more than an order of magnitude higher than that of control devices without the NiO interlayer. The on/off current ratio surpasses 10^3, enabling effective voltage modulation under 1550 nm illumination. These enhancements are attributed to suppressed trap-assisted recombination, optimized band alignment and improved carrier extraction efficiency, as confirmed by bias-dependent photoresponse measurements, capacitance-voltage profiling, and deep-level transient spectroscopy (DLTS). Notably, ALD provides sub-nanometer thickness control and exceptional conformality even on rough, solution-processed CQD films, capabilities unattainable by conventional deposition techniques such as sputtering or evaporation.

This work establishes a generalizable strategy for interface-engineered performance optimization in solution-processed optoelectronics, paving the way toward high-performance, scalable fabrication of CQD-based electronic and photonic devices.

AA-TuP-41 Preventing Plasma Damage in Plasma Enhanced Atomic Layer Processing*, Joe Alex, Birol Kuyel,* NANO-MASTER, Inc.

This study investigates plasma-induced defect formation in plasma-enhanced Atomic Layer Deposition (ALD) and Atomic Layer Etching (ALE) processes in the hybrid ALD/ALE system, with a focus on mitigating damage to thin-film structures. We evaluate the architecture of the Nano-Master NLD-4000 ALD system's plasma termination assembly in reducing ion-induced surface and subsurface defects. Film cross-sections are analyzed using scanning electron microscopy (SEM) to quantify structural degradation under conventional plasma exposure and compare it with damage levels achieved using the NLD-4000 architecture. We demonstrate the reduction or complete elimination of the plasma-induced damage, highlighting the role of the unique chamber design in enabling damage free Plasma enhanced ALD/ALE processes.

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