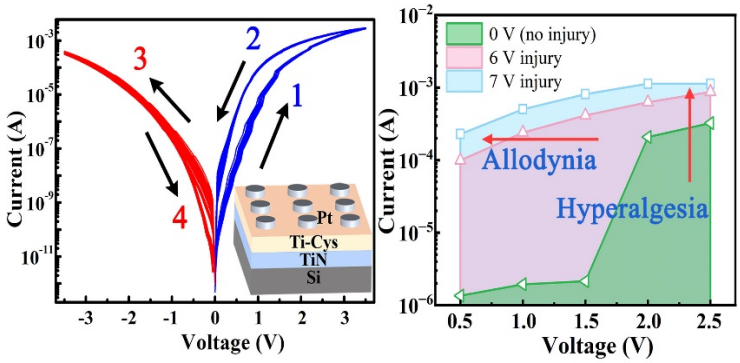

Fig. 1. (a) I–V curves of the Pt/Ti-Cys/TiN device for 100-cycle DC ramped voltage tests. The schematic of this hybrid device is shown in the inset. (b) The maximum output currents in log scale at 2 ms voltage pulses with different amplitudes after different injury pulses.

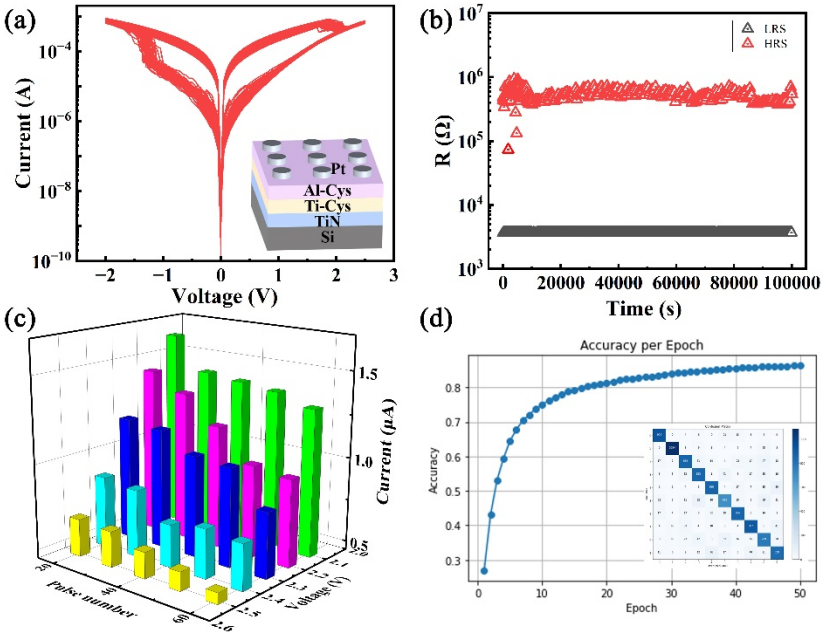

Fig. 2. (a) I-V curves for 100 tests with the schematic of the bilayer Pt/Al-Cys/Ti-Cys/TiN memristor device. (b) Retention of the bilayer memristor for 10^5 s. (c) Response of a memristor device to different pulse programs. (d) Training epoch-dependent recognition accuracy and the confusion matrix.