Tuesday Evening, June 24, 2025

ALD Applications
Room Event Hall - Session AA-TuP
ALD Applications Poster Session

AA-TuP-1 The Role of Al2O3 ALD Coating on Sn-Based Intermetallic Anodes for Rate Capability and Long-Term Cycling in Lithium-Ion Batteries, ***Niloofar Soltani,*** *Amin Bahrami, Daria Mikhailova, Kornelius Nielsch,* Leibniz Institute for Solid State and Materials Research, Germany

The electrochemical performances of CoSn2 and Ni3Sn4 as potential anode materials in lithium-ion batteries (LIBs) are investigated using varying thicknesses of an alumina layer deposited by the atomic layer deposition (ALD) technique. Rate capability results showed that at high current densities, Al2O3-coated CoSn2 and Ni3Sn4 electrodes after 10-ALD cycles outperformed uncoated materials. The charge capacities of coated CoSn2 and Ni3Sn4 electrodes are 571 and 134 mAh g−1, respectively, at a high current density of 5 A g−1, while the capacities of uncoated electrodes are 363 and 11 mAh g−1. When the current density is reduced to 1 A g−1, however, the cycling performances of Al2O3-coated CoSn2 and Ni3Sn4 electrodes fade faster after almost 40 cycles than uncoated electrodes. The explanation is found in the composition of the solid-electrolyte interface (SEI), which strongly depends on the current rate. Thus, X-ray photoelectron spectroscopy analysis of SEI layers on coated samples cycles at a low current density of 0.1 Ag−1, revealed organic carbonates as major products, which probably have a low ionic conductivity. In contrast, the SEI of coated materials cycled at 5 Ag−1 consists mostly of mixed inorganic/organic fluorine-rich Al-F and C-F species facilitating a higher ionic transport, which improves electrochemical performance.

AA-TuP-2 ALD on Particulate Materials: A Data-Driven Review of Technologies, Materials and Applications from the Bottom Up, ***Peter M. Piechulla,*** *Mingliang Chen,* Delft University of Technology, Netherlands*; Riikka L. Puurunen,* Aalto University, Finland*; J. Ruud van Ommen, Aris Goulas,* Delft University of Technology, Netherlands

The most prominent application of ALD today is semiconductor manufacturing using wafer-based processes, although some of the earliest fundamental ALD studies were carried out on particles. However, ALD on particulate materials (ALDpm) remained a comparably small research area over several decades, and only gained momentum recently, when researchers recognized its ability to tailor nanomaterials (thin films, nanoparticles) with atomic-level control as a valuable trait for a number of particle-based applications. While thermocatalysis was the initial driver of research, and still is important today, drastic innovations to the respective industrial processes are difficult to introduce. New drivers of ALDpm research are highly innovative application fields such as energy conversion (i.e. electrocatalysis) and storage (batteries), where the disruptive potential of ALDpm technology has been recognized in previous application-centered review articles[1].

Here, we cast a broader view on the field. First, we identified approximately 800 original research articles on ALDpm[2], with the key qualification that particles remain in dispersible form after the process. Previous review work[3] had shown the following main categories as defining for ALDpm: reactors, precursor chemistry, support materials, process conditions and properties of coated material. In a second step, we aggregated key qualitative and quantitative data from every article for each of these categories into a single dataset (reduced version online)[2]. Third, we perform a bottom-up analysis of the field of ALDpm by systematic categorization and statistical analysis of the dataset. This includes, e.g., the different reactor engineering approaches to address the challenges of processing particulate substrates, substrate materials, coated materials, and processing conditions. While being agnostic about applications during article screening, we also provide an overview of recent and popular applications. In summary, this review provides both new inspiration for potentially high-volume, high-value applications, and an overview of technologies available to perform ALDpm.

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AA-TuP-3 Atomic Layer Deposition of Silver Catalysts for Hydroxide Exchange Membrane Fuel Cells, ***Gwon Deok Han,*** Sookmyung Women's University, Republic of Korea*; Beum Geun Seo,* Korea University, Republic of Korea*; Hyung Jong Choi,* Stanford University*; Junmo Koo,* Korea Maritime & Ocean University, Republic of Korea*; Fritz Prinz,* Stanford University*; Joon Hyung Shim,* Korea University, Republic of Korea

Hydroxide exchange membrane fuel cells (HEMFCs) are an emerging class of low-temperature fuel cells. A key advantage of HEMFC technology is its operation under alkaline conditions, which enables the use of non-platinum group metals (non-PGMs) as catalysts for fuel cell reactions. In contrast, proton exchange membrane fuel cells (PEMFCs), widely used in fuel cell electric vehicles (FCEVs), require the use of expensive platinum group metals (PGMs). Thus, the development of HEMFCs plays a crucial role in accelerating the growth of the FCEV market.

Silver has been investigated as a promising catalyst for HEMFCs due to its catalytic activity and durability in alkaline environments. Moreover, given its cost-effectiveness compared to platinum, silver catalysts offer a viable solution for significantly reducing the high production costs of FCEVs. Recent studies have proposed various methods for preparing silver catalysts as HEMFC cathode materials. However, there remains ample room for enhancing the electrochemical performance of HEMFCs through the rational design of silver catalysts.

Here, we demonstrate for the first time that an atomic layer deposition (ALD)-based silver catalyst applied to the HEMFC cathode can achieve high fuel cell performance. We successfully coated silver nanoparticles uniformly onto porous carbon nanotubes using plasma-enhanced ALD. The ultralow loading of silver catalysts enabled by ALD contributes to achieving power density exceeding 2 kW/mg_{Ag} in an alkaline environment. This study highlights the potential of ALD as an effective approach for fabricating fuel cell catalysts.

AA-TuP-4 A Study on the Development of a New Ga Precursor for IGZO Thin Films and the Characteristics of Thin Films Using the Same, ***kyung-eun Lee,*** *Min-hyuk Nim, Taek Seung Yang,* lakematerials, Republic of Korea

New Ga precursors containing -F and -Cl were synthesized, and their reactivity was confirmed. The physical properties of two of these precursors were confirmed. ALD deposition evaluation was performed using these precursors, and the ALD window was confirmed at 160-220 ° C. The deposition result was analyzed using XPS, and step coverage was confirmed through deposition using Trench wafer.

AA-TuP-5 A Study on the Characteristics of Thin-Film Using New in Producers for IGZO Thin-Film, ***HAN-BOM KIM,*** *MIN-HYUK NIM, Taek Seung Yang,* lakematerials, Republic of Korea

The characteristics of ALD thin films were investigated using a newly developed liquid indium (In) precursor. The ALD window was identified within the temperature range of 160–200°C, and the film composition was analyzed using X-ray photoelectron spectroscopy (XPS). Additionally, step coverage was evaluated through deposition on a trench wafer.

AA-TuP-6 A Study on the Characteristics of IGZO Thin Films Using New Ga and In Precursors, ***Yeon-Soo Kim,*** *Kyung-Eun Lee, Min-Hyuk Nim, Taek Seung Yang, Chang Ho Song,* LAKE MATERIALS CO., LTD., Republic of Korea*; Nam Eun Kim, Ki-Seok An,* KRICT, Republic of Korea

In this study, we investigated the properties of IGZO thin films using novel Ga and In precursors for the development of next-generation IGZO materials. During the deposition process, DADI and DATI (L2i-8) were used as In precursors, Ga-009 and Ga-026 as Ga precursors, and DEZ as the Zn precursor. These precursors were deposited via atomic layer deposition (ALD) with an In:Ga:Zn composition ratio of 1:1:1. The composition of the deposited IGZO films was analyzed using X-ray photoelectron spectroscopy (XPS), and their mobility characteristics were measured. Based on these results, we identified the optimal precursor combination for IGZO thin films and evaluated their potential application in next-generation high-performance thin-film transistors (TFTs). This study is expected to contribute to the enhancement of IGZO thin-film performance and their application in advanced electronic devices.

AA-TuP-7 Effect of Al_2O_3 Passivation Layer on Atomic Layer Deposited ZnSnO and Al-doped ZnSnO Thin-Film Transistors with Remarkable Bias-Stress Stability, ***Jinheon Choi,*** *Sahngik Mun, Juneseong Choi, Jaewon Ham, Hyungjeung Kim, Shihyun Kim, Subin Moon, Cheol Seong Hwang,* Seoul National University, Korea (Democratic People's Republic of)

Dynamic random-access memory (DRAM) has followed the direction of increasing integration density, and the cell structure may change from a

planar configuration to a three-dimensional (3D) configuration. The stacked cell structure of 3D DRAM requires channel materials for each layer, rendering silicon substrates impractical. Therefore, amorphous oxide semiconductors (AOSs) are feasible candidates due to their excellent uniformity, low leakage current, reasonable mobility (~10 cm^2/Vs), and ability to be deposited by atomic layer deposition (ALD). For 3D DRAM structure, a passivation layer is essential to isolate cells and prevent chemical reactions between AOSs and the ambient environment. Still, AOS properties are significantly influenced by subsequent processing steps, particularly the diffusion of ubiquitous mobile hydrogen. Diffused hydrogen can induce a negative shift of threshold voltage (V_{th}) of thin-film transistors (TFTs), leading to increased power consumption and degrading negative/positive gate bias stress (NBS/PBS) stability. Thus, detailed mechanisms of adopting passivation layers and their optimization are critical for designing effective TFTs in 3D DRAM applications.

This study investigates a new mechanism for the impact of passivation layers on amorphous zinc tin oxide (*a*-ZTO) and Al-doped *a*-ZTO (*a*-AZTO) thin films and their corresponding TFTs and demonstrates optimized properties. Unoptimized passivation layers increased the hydrogen content in *a*-ZTO, leading to a significant V_{th} in the negative voltage direction. Conversely, optimized passivation mitigated hydrogen penetration but caused oxygen deprivation of *a*-ZTO, which still led to a large negative V_{th}. In contrast, for *a*-AZTO TFTs, the pre-existing Al-O bonds in the channel minimized oxygen deprivation, leading to negligible V_{th} variations. Nevertheless, hydrogen diffusion through a HfO_2 gate insulator persisted even under optimized passivation conditions, causing an abnormal hump during PBS tests. Replacing the gate insulator with Al_2O_3 effectively eliminated this anomaly. Finally, using a 10-nm-thick Al_2O_3 gate insulator and indium-tin-oxide source/drain electrodes demonstrated optimized TFT characteristics for 3D DRAM: V_{th} of -0.12 V, field-effect mobility of 10.12 cm^2/Vs, subthreshold swing (SS) of 135 mV/decade, and minimal V_{th} shifts of -15 mV, 1 mV during 1000 s of NBS, PBS tests, respectively.

AA-TuP-8 Ferroelectric-Like Tunnel Switch Behavior of an Antiferroelectric/Dielectric $Hf_{1-x}Zr_xO_2/Al_2O_3$ Bilayer Structure, ***Seungheon Choi***, *Seungyong Byun, Han Sol Park, Cheol Seong Hwang,* Seoul National University, Republic of Korea

Ferroic heterostructures have recently emerged as a key methodology for developing advanced ferroic devices. Among them, ferroelectric (FE) and antiferroelectric (AFE) nanolaminate structures have demonstrated improved ferroelectric properties, such as higher remanent polarization (P_r) and lower coercive field (E_c).[1] Furthermore, scaling these structures has shown promise for capacitance-boosting effects due to ferroelectric negative capacitance in direct integration with semiconductor channel structures.[2]

The devices with integrated (anti)ferroelectric complex heterostructures require a systematic understanding of the behaviors of the individual layers and the electrostatic interactions between them. As a preliminary step, this study investigates the unique electrical behavior of AFE/dielectric (DE) bilayer systems, which is crucial for understanding the complex behavior of FE-AFE heterostructures because AFE and FE materials inherently possess dielectric properties.

Specifically, $Hf_{1-x}Zr_xO_2$ thin film exhibiting strong AFE characteristics was deposited using thermal atomic layer deposition, and this film demonstrates ferroelectric-like switching behavior when in direct contact with Al_2O_3 thin film. This bilayer structure shows tunnel-switch behavior similar to that observed in the FE/DE bilayer.[3]

Ferroelectric polarization switching in FE/DE bilayers induces a large internal field, making the dielectric layer susceptible to tunneling. Consequently, charges are trapped at the FE/DE interface, compensating the ferroelectric bound charge. Similarly, in AFE/DE bilayers, interface-trapped charges compensate for spontaneous polarization induced by external bias. Unlike a typical AFE single-layer capacitor, where metal electrode charges are free to move, the trapped charges in the AFE/DE structure are less mobile when the bias is removed. This behavior prevents the AFE layer from back-switching to a non-polar state, and only when a reverse bias is applied can the trapped charge tunnel out, enabling switching. This results in a macroscopic tunnel-switch behavior, distinct from conventional AFE pinched loop hysteresis.

These findings challenge the conventional understanding of antiferroelectricity and emphasize the importance of AFE/DE bilayer as a step toward more complex heterostructures and AFE-based devices. By building a stepwise understanding of these interactions, this work lays the groundwork for advancing next-generation ferroic devices and optimizing their performance.

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AA-TuP-9 Demonstration of Amorphous Oxide Semiconductor Thin Film Transistors with Mold Structure via Channel-Last Process, *Cheol Seong Hwang,* ***Subin Moon****, Sukin Kang, Jinheon Choi, Sahngik Aaron Mun, Juneseong Choi, Jaewon Ham, Hyungjeung Kim, Shihyun Kim,* Seoul National University, South Korea

Three-dimensional dynamic random-access memory (3D DRAM) offers significant potential to enhance memory density and performance through vertically integrated cell architectures. Among various channel materials, amorphous oxide semiconductors (AOSs) have emerged as promising candidates due to their compatibility with atomic layer deposition (ALD), which enables precise and conformal deposition even on 3D structures. Also, AOS materials exhibit feasible electron mobility (~10 $cm^2V^{-1}s^{-1}$), high uniformity, and low leakage current. However, the electrical characteristics of AOS thin-film transistors (TFTs) can be degraded when adopted to 3D DRAM. When the channel is deposited at the early stages of fabrication, hydrogen incorporation[1] and plasma-induced damage[2] during multi-layer stacking deteriorate TFTs' electrical stability and switching characteristics. Even though several strategies have been proposed to address these issues, an optimal solution for reliably integrating AOS into stacked-layer designs remains challenging.

This study introduces a novel strategy using mold structures that deposit channel materials as a late step to prevent the degradation of AOS characteristics. To define the mold structure, a tungsten sacrificial layer was utilized to define the channel volume, followed by selective tungsten recess to form a SiO_2 mold. Subsequently, an amorphous ZnSnO (a-ZTO) channel was deposited within the predefined empty region of the mold. This approach allows the AOS channel to be deposited after constructing structures, effectively preventing hydrogen incorporation, plasma-induced damage and high-temperature treatments known to degrade material properties. TFTs fabricated within the mold structure demonstrated threshold voltage, saturation mobility and subthreshold swing of -0.13 V, 5.37 $cm^2V^{-1}s^{-1}$, and 230 mV/decade, respectively. These results, comparable to those measured in conventional a-ZTO TFTs[3], confirmed that this approach preserves the intrinsic characteristics of AOS, achieving stable switching performance and reliable device operation.

AA-TuP-10 Utilizing Ethanol as a Pre-reducing Agent for Atomic Layer Deposition MoO_2/TiO_2-Based Metal-Insulator-Metal Capacitors to Enhance Electrical Properties, ***Soomin Yoo****,* Kyunghee University, Republic of Korea*; Seungwoo Lee,* Kyunghee Univerity, Republic of Korea*; Chaeyeong Hwang, Woojin Jeon,* Kyunghee University, Republic of Korea

Metal-insulator-metal (MIM) structures, such as capacitors in DRAM devices, play a critical role in determining the operating characteristics of various memory semiconductors. [1] To enhance the performance of such devices, it is essential to achieve high capacitance in MIM capacitors. Among the various high dielectric constant (*k-value*) materials, TiO_2 is the most promising dielectric because it has a very high dielectric constant of 170 when in a rutile crystalline structure.[2] To obtain rutile TiO_2, an electrode with crystallographic similarity used such as MoO_2 or Ru. In the case of employing MoO_2 as the electrode, MoO_2 is initially deposited in the form of higher oxidation state of MoO_x ($2<x<3$)on a TiN electrode and followed by a thermal annealing process to induce the reduction of MoO_x to MoO_2 through the oxygen scavenging effect of TiN. During this reduction process, a severe morphology degradation of MoO_2 is observed which is induced by simultaneous reduction and crystallization process occur.[3] This morphology degradation of MoO_2 would induce degradation in crystallinity and morphology of TiO_2 thin film deposited on the MoO_2. To prevent morphology degradation during the reduction from of $MoO_x$to MoO_2 and TiO_2 of dielectric layer, a reducing agent was introduced into the MoO_2 ALD process to pre-reduction MoO_x before to crystallization.

In this study, ethanol was introduced after the Mo precursor feeding step, allowing the pre-reduction of MoO_x before the subsequent oxidation step. This approach effectively modulates the oxidation state of MoO_x. First, we compared the oxidation states of Mo ion in the as-deposited thin films using X-ray photoelectron spectroscopy analysis. As a result, the Mo^{6+} ratio

in EtOH-treated MoO_x decreased, indicating that the MoO_x thin film was pre-reduced through ethanol treatment. This result well coincides with the X-ray diffraction result of the as-deposited state, indicating that the proportion of the intermediate phase Mo_4O_{11} increased due to the pre-reduction effect after ethanol treatment. Furthermore, atomic force microscopy analysis confirmed the improvement in the morphology of TiO_2 deposited on ethanol-treated MoO_2.

References

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AA-TuP-11 Nontemplate *in-Situ* Crystallization of Atomic Layer Deposited Molybdenum Dioxide *via* Substitutional Doping of Ruthenium*, Chaeyeong Hwang,*** Kyunghee university, Republic of Korea*; Myeong Ho Kim, Yoon-A Park, Jin-Sik Kim,* R&D Team 1, UP Chemical Co., Ltd., Republic of Korea*; Woojin Jeon,* Kyunghee University, Republic of Korea

Rutile-phased TiO_2, with its high dielectric constant (~170), is a promising insulator for next-generation metal-insulator-metal (MIM) capacitors [1]. However, due to its thermodynamically high-temperature stable phase, thermal annealing within the actual devices process temperature limits is insufficient for crystallization. Consequently, extensive research has focused on utilizing the template effect, through structural similarity with bottom electrodes to facilitate crystallization. Among various candidates, MoO_2 has emerged as a promising material due to its high work function (~5.8 eV), and superior redox stability [2,3]. A previous study showed that MoO_2 crystallization can be achieved by ALD MoO_x ($2 < x < 3$) on TiN, the utilizing TiN's oxygen scavenging to form rutile TiO_2 and induce the template effect [3].

While promising for mass production, MoO_2 requires a TiN/MoO_2 stacked electrode, increasing the proportion of the bottom electrode within the capacitor thickness limits. This, reduces the thickness of the TiO_2 insulator, exacerbating leakage current concerns due to the small bandgap of TiO_2.

To address this limitation, crystallization technique of MoO_2 on SiO_2 substrates is required. However, in the absence of the oxygen scavenging and template effect, the crystallization temperature of MoO_2 is inevitably higher on SiO_2. This presents a significant challenge as MoO_3, a component of MoO_x ($2 < x < 3$), undergoes sublimation at 550℃ [4]. Consequently, crystallization leads to severe mass loss, resulting in a discontinuous MoO_2 thin film with exposed SiO_2, which interferes with MIM capacitor formation.

In this study, we adopted Ru doping to facilitate MoO_2 crystallization on SiO_2 while maintaining its applicability as a MIM capacitor film. Increasing Ru concentration reduced the crystallization temperature of MoO_2, ultimately enabling as-deposited crystallization. Comprehensive analyses confirmed that Ru-doped MoO_2 successfully induced rutile TiO_2 formation, verifying its suitability as an electrode.

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AA-TuP-12 Comprehensive Study on ALD HfO_2-based RRAM with Next-Generation Ru Electrodes for High-Performance Memory Technology*, Yunsur Kim, Jiyong Woo,* Kyungpook National University, Republic of Korea

Emerging memory technologies are gaining significant attention as researchers seek to revolutionize the existing memory hierarchy. These technologies, which rely on resistance-based data storage, include phase change memory (PCM), magnetoresistive random access memory (MRAM), ferroelectric random access memory (FeRAM), and resistive random access memory (RRAM). Among them, RRAM stands out due to its fast switching speed, low power consumption, sub-10 nm scalability, long endurance, and potential for non-volatile storage and neuromorphic computing.

RRAM operates by modulating resistance through the formation and rupture of a conductive filament (CF) within a metal oxide layer. When the applied voltage exceeds a threshold, oxygen vacancies (V_0) migrate and form a CF, resulting in a low resistance state (LRS). Reversing the voltage disperses the V_0, rupturing the CF and restoring a high resistance state (HRS). This resistive switching behavior has been extensively studied in binary metal oxides such as hafnium oxide (HfO_x), titanium oxide (TiO_x), tantalum oxide (TaO_x), and aluminum oxide (AlO_x) due to their compatibility with the CMOS back-end-of-line (BEOL) process.

The deposition method for the switching layer significantly impacts RRAM performance. Common techniques include pulsed laser deposition (PLD), atomic layer deposition (ALD), and reactive sputtering. ALD is favored for its precise thickness and uniformity control, ensuring reliable device characteristics.

Electrode selection also plays a crucial role, affecting switching speed, endurance, and retention. Conventional electrodes include Al, Ti, Cu, and W, but noble metals such as Ru, Ir, and Pt are being explored for improved performance. Among them, Ru is of particular interest due to its high work function (~4.7 eV), low resistivity (7 μΩ·cm), and strong chemical stability, enhancing RRAM reliability.

In this study, we investigated the resistive switching properties of HfO_x-based RRAM with different stack configurations. We compared RRAMs with a stoichiometric HfO_2 layer deposited via ALD and a sub-stoichiometric HfO_x layer formed by sputtering. Additionally, we examined the impact of various electrode materials, including W, Ti, Ta, and Ru. The ALD-HfO_2-based RRAM with a Ru bottom electrode exhibited superior endurance, excellent cycle-to-cycle uniformity, and high device-to-device uniformity. These findings highlight the importance of optimizing both the switching layer and electrode material for high-performance RRAM applications in next-generation memory and neuromorphic computing.

AA-TuP-13 Effect of the Number and Distribution of Al_2O_3 Atomic Layer Deposition Cycles Within Hfo_2 Layer on Ferroelectric Characteristics*, Hyoungjin Park, Jiyong Woo,* School of Electronic and Electrical Engineering, Kyungpook National University, Republic of Korea

Since the 1990s, extensive research has been conducted on ferroelectric devices, which are considered emerging candidates that can replace the conventional charge-based memory devices. The spontaneous polarization of these materials, commonly observed in ternary perovskite compounds such as $BaTiO_3$, $PbZr_xTi_{1-x}O_3$, and $Sr_2Bi_2TaO_9$, results from the rapid reorientation of dipoles, enabling fast switching speeds and excellent endurance characteristics. However, the practical application of these materials is hindered by their complex chemical composition, which lacks compatibility with standard semiconductor fabrication processes, as well as the requirement for relatively thick films (>100 nm) to achieve stable polarization. Recently, thin HfO_2 films have garnered significant attention due to their remarkable ferroelectric properties. These properties originate from the formation of a specific orthorhombic (o) crystalline phase, induced by high-temperature annealing. However, because the o-phase is thermodynamically unstable, strategies such as dopant incorporation and post-metallization annealing, which introduce global strain, have been employed to enhance its stability. Studies have demonstrated that ferroelectricity in HfO_2 can be realized through doping with elements such as Si, Zr, and Al, followed by high-temperature annealing. Among these, Al-doped HfO_2 (Al:HfO_2) has been widely investigated due to its excellent thermal stability and reduced leakage current, attributed to its wide energy bandgap. The fabrication of Al:HfO_2-based ferroelectric devices commonly involves atomic layer deposition (ALD), where Al_2O_3 layers are periodically introduced into HfO_2 films to incorporate Al dopants. Prior research has focused on optimizing ALD process parameters for HfO_2 and Al_2O_3 to enhance ferroelectric properties from a fabrication standpoint. In addition, advanced annealing techniques have been explored to promote crystallization at lower temperatures and stabilize the o-phase by controlling the cooling process. Beyond annealing optimization, interfacial engineering strategies have been developed to sustain the o-phase, such as integrating an additional dielectric layer within doped HfO_2 films or modifying the ferroelectric/electrode interface. Despite these advancements, most studies assume a uniform dopant distribution throughout the HfO_2 layer. In this work, we systematically investigate the impact of Al_2O_3 distribution within the HfO_2 matrix on ferroelectric performance. Furthermore, we demonstrate that asymmetric doping, wherein Al dopants are concentrated primarily in the bottom region of the HfO_2 layer, leads to enhanced polarization characteristics.

AA-TuP-14 Atomic Layer Deposited Single-Atom Catalysts of Pt/Co3O4 for Improved Electrocatalytic Hydrogen Evolution Reaction Performance*, Yue Huang, Ying-Jie Ma, Ai-Dong Li,* Nanjing University, China

Atomic layer deposition (ALD) technique enables precise control over material synthesis at the atomic scale, which has been successfully employed to design and fabricate single-atom catalysts. In contrast to traditional catalyst synthesis methods, the self-limiting nature of ALD ensures the production of catalysts with monodisperse sizes and uniform distribution on the support, leading to enhanced catalytic activity, selectivity, and stability. Furthermore, the ALD process results in minimal

contamination from residual salts, therefore it is urgent to develop ALD-derived single-atom catalysts and their catalytic properties.

In this study, ALD was explored to regulate the pulse time of the platinum precursor in the chamber, thereby controlling the uniform dispersion of Pt atomic catalysts on Co_3O_4 support. Isolated metallic Pt atoms directly bonded to the support. The metal atom-support interaction generated charge transfer between them, which greatly modulated its electronic and catalytic properties. We evaluated the performance of single-atom Pt/Co3O4 catalysts.Interestingly, the catalyst demonstrated strong hydrogen evolution reaction (HER) activity under alkaline conditions, exhibiting a remarkably low overpotential of only 34 mV at 10 mA cm^{-2} (Figure 1). Furthermore, the interaction between the Pt single atoms and the Pt-O-Co bond interface enhances the stability of the catalyst surface, preventing aggregation or cluster formation, which contributes to an extended catalyst lifespan. Our results provide a new way to develop efficient and stable single-atom electrocatalytic materials using ALD.

AA-TuP-15 Atomic Layer Deposited Amorphous High-entropy Oxide Protective Layer for Stable Zinc Metal Anode, *Li-Ling Fu,* ***Ai-Dong Li,*** Nanjing University, China

Aqueous zinc ion batteries (ZIBs) have attracted much attention in the field of future large-scale energy storage, with the advantages of high theoretical capacity (820 mAh/g and 5855 mAh/cm^3), low reduction potential (-0.76 V), high safety and low cost. However, dendrites and side reactions on the surface of the zinc metal anode greatly limit the cycling stability of zinc ion batteries. To address this problem, an effective method is to construct an artificial protective coating on the surface of the zinc anode.The preparation of conventional single metal oxide coating materials using atomic layer deposition (ALD) processes can inhibit zinc dendrite generation to some extent. However, unitary, binary or ternary oxides are many times insufficient to address the various challenges in zinc ion batteries.

In this work, inspired by the concept of high entropy, we constructed $TiYZrAlSnO_x$ amorphous high-entropy oxides (HEOs) coatings on the surface of zinc anode by atomic layer deposition (ALD) as shown in Fig. 1. This high-entropy oxide electrode has abundant zinc-friendly sites due to the cocktail effect generated by mixing various zinc-friendly elements with corrosion-resistant elements, which promotes uniform zinc deposition and suppresses zinc dendrites and by-products on the zinc anode surface. Moreover, this high-entropy oxide enhances the migration kinetics of Zn^{2+}, facilitates the desolvation process of Zn^{2+}, and reduces the zinc deposition energy barrier.

In addition, this amorphous high-entropy oxide coating can effectively inhibit the hydrogen precipitation reaction and reduce the generation of by-products. As a result, this Zn@HEOs anode exhibits excellent cycling stability more than 4000 h at 5 mA cm^{-2} and 1 mAh cm^{-2}. Compared with the conventional high-entropy oxide preparation process, this work combined with ALD technology to realize an amorphous high-entropy oxide protective layer on the surface of zinc anode at low temperature, which provides an alternative strategy to achieve a stable zinc metal anode.

AA-TuP-16 Transforming Waste Textiles into VC/V_2O_{3-x}-Decorated Porous Carbon for Flexible Battery Hosts, ***Viet Phuong Nguyen,*** *Seung Mo Lee,* Korea Institute of Machinery & Materials (KIMM), Republic of Korea

In this study, we present a sequential synthesis approach combining V_2O_5 atomic layer deposition with subsequent carbothermic reduction to transform waste textiles into porous, flexible carbon textiles uniformly decorated with VC/V_2O_{3-x} hybrid nanoparticles. This innovative material serves as a robust and flexible host for both sulfur cathodes and lithium metal anodes in flexible Li–S batteries. The defective V_2O_{3-x} component effectively traps polysulfides, while the conductive VC phase catalytically promotes their fragmentation. Additionally, the well-dispersed VC/V_2O_{3-x} nanoparticles act as lithiophilic sites, facilitating uniform lithium nucleation and suppressing dendrite growth. As a result, the full cell exhibits outstanding rate performance (882 mAh g^{-1} at 5 C) and an exceptionally low capacity decay rate of 0.02% per cycle over 1000 cycles at 1 C. Even at a high sulfur loading of 7.0 mg cm^{-2}, the battery achieves a remarkable areal capacity of 6.29 mAh cm^{-2} at 0.2 C. This work offers an effective strategy to simultaneously mitigate the polysulfide shuttle effect and lithium dendrite formation, paving the way for high-performance, flexible Li–S full batteries.

AA-TuP-17 Dual Ferroelectric Stack by ALD with Tunable Coercive Voltage for High-Density 3D Memory Applications, *Jiyong Woo,* ***Jiae Jeong,*** Kyungpook National University, Republic of Korea

Doped HfO_2-based thin films have been regarded as promising material for non-volatile memories due to their scalability and complementary metal-oxide-semiconductor compatibility. To induce the ferroelectricity in HfO_2 film, a specific dopant needs to be incorporated into the HfO_2 layer, followed by a high-temperature annealing process, which enables the formation of an orthorhombic phase. This structural transformation facilitates the generation of permanent dipoles, allowing the HfO_2 dielectric layer (DL) to transform into a ferroelectric layer (FL). Among various dopant candidates, Zr-doped HfO_2 (HZO) has attracted attention because the orthorhombic phase in HZO can be achieved at a relatively low temperature (400 ℃) while exhibiting a high remnant polarization (P_r).

Due to its low thermal budget, HZO is considered a strong candidate to replace conventional charge-trap approaches in 3D ferroelectric NAND applications. In a ferroelectric field-effect transistor structure, where the HZO FL is positioned between the gate and oxide channel layers, applying a gate voltage aligns the dipoles within the FL either the downward or upward direction. This dipole reorientation modulates the threshold voltage (V_T) by either attracting or repelling electrons at the channel interface, creating a memory window (MW) in transfer characteristics. Consequently, MW is created by the difference between high and low V_T. Fine-tuning multilevel V_T states can be obtained within the MW is crucial for enhancing memory density. The V_T range is primarily determined by the coercive voltage (V_C) of FL. While previous research has confirmed that the HZO FL exhibits a high P_r due to abrupt polarization switching at V_C, it has also been observed that the V_T remains unchanged even at higher voltages. Various approaches have been explored to enhance V_C, including incorporating an Al_2O_3 DL within the HZO FL or constructing dual-layer HZO FL structures with varying thicknesses.

In this study, we focus on investigating ferroelectric properties by examining the relationship between ramping voltage and V_C modulation, P_r control. Furthermore, our findings provide insights into applications where precise adjustments of P_r and V_C in ferroelectric capacitors are required. This adjustability is achieved through the sequential stacking of heterogeneous FLs, where each layer is deposited using atomic layer deposition (ALD). Specifically, Al-doped HfO_2, which exhibits more gradual polarization switching at V_C, was integrated with HZO. Through the synergistic interaction between the heterogeneous FLs, we successfully tuned P_r values from 1 to approximately 20 μC/cm^2 while varying V_C from 1 to 3 V.

AA-TuP-18 Inducing the Tetragonal-Phase HfO_2 in ZrO_2/HfO_2 Stack by Introducing the Controlled Interfacial Layer, ***Woo Young Park,*** WONIKIPS, Republic of Korea

ZrO_2 and HfO_2 have been employed as insulators in dynamic random access memory (DRAM) capacitor and gate dielectric applications. Moreover, HfO_2 was introduced to the ZrO_2/HfO_2 laminated structure for enhancing the dielectric constant (*k*) because it was reported that tetragonal-phased HfO_2 has a *k* value of 46.9. In this regard, various results for achieving a tetragonal-phased HfO_2 thin film deposition process have been reported. However, the formation of a polymorph of the HfO_2 thin film, the monoclinic phase, was inevitable. Furthermore, the crystal composition of HfO_2, a ratio of tetragonal and monoclinic phases, is strongly affected by the film thickness, resulting in a severe k value change in HfO_2 thin film depending on its thickness. This *k* value change of HfO_2 makes it hard to obtain a designated *k* value of ZrO_2/HfO_2 laminated structure by controlling the HfO_2 layer thickness.

In this paper, we introduced a “controlled interfacial layer (CIL)” for suppressing the changing of the *k* value of the HfO_2 layer depending on its layer thickness in the ZrO_2/HfO_2 laminated structure. The newly introduced CIL allows to maintain the Tetragonal phase of HfO2 even if the thickness of the HfO2 layer increases in a given ZrO2/HfO2 stack structure. Consequently, relatively high and constant *k* values of HfO_2 were obtained in the various ZrO_2/HfO_2 laminated structures. Finally, an optimized ZrO_2/HfO_2 laminated structure with the CIL was investigated for the DRAM capacitor dielectric application.

AA-TuP-19 Boosting SERS Performance of Moo_3 Substrates via ALD Surface Modifications, ***Yanqiang Cao,*** *Wenyue Yin,* Nanjing University of Science and Technology, China

Surface Enhanced Raman Scattering (SERS) has emerged as a highly potent analytical technique, finding extensive applications in chemical and biological sensing, primarily attributed to its remarkable sensitivity and distinct molecular fingerprinting capabilities. Among a diverse array of SERS substrates, MoO_3 based materials have garnered substantial attention owing to their unique semiconductor characteristics and great potential for high performance SERS applications. Nevertheless, the inherent SERS performance of MoO_3 substrates frequently requires enhancement to satisfy the demands of practical applications.

In this research, the surface of MoO_3 was treated using Atomic Layer Deposition (ALD) technology, leading to a notable improvement in the SERS performance of the MoO_3 substrate. By depositing a thin and uniform layer of Al_2O_3 along with hydroxyl functional groups on the surface of MoO_3, the charge separation efficiency within the MoO_3@Al_2O_3 composite was significantly enhanced, approximately doubling the SERS performance of orthorhombic MoO_3. Subsequently, the MoO_3@$Al_2(MoO_4)_3$ heterojunction was fabricated through a calcination process, further augmenting the SERS performance of the MoO_3 substrate. Ultimately, a SERS substrate with high sensitivity, excellent uniformity, and remarkable stability was successfully developed.

During the exploration of the SERS performance enhancement mechanism, it was discovered that the SERS performance of the MoO_3@Al_2O_3 substrate, both before and after calcination, exhibited a strong correlation with the thickness of the ALD deposited Al_2O_3 coating. The modified MoO_3 substrate and the MoO_3@$Al_2(MoO_4)_3$ heterojunction substrate demonstrated a detection limit of 10^{-8} M for methylene blue (MB) molecules and retained excellent SERS performance even after 90 days. Through precise control of the ALD cycle number of Al_2O_3, we systematically investigated the impact of the Al_2O_3 thickness on the SERS performance of the substrate, thereby deepening our understanding of the strategies for enhancing the performance of semiconductor based SERS substrates.

AA-TuP-20 ZrO_2 Seed-layer Induced Crystallization of $Hf_{1-x}Zr_xO_2$ with Energy Barrier Lowering Effect of the Ferroelectric Orthorhombic Phase Transition, ***Kyongjae Kim***, *Eunseo Jo, Myeonggeun Yoo, Youseung Rim,* Sejong University, Republic of Korea

Ferroelectric $Hf_{1-x}Zr_xO_2$ has garnered significant for the next generation of non-volatile memory material, architecture and logic circuits.For materials to integrate to devices, research of ferroelectric $Hf_{1-x}Zr_xO_2$ has been studied terms of the controllability of dopants, strain, surface energy, and oxygen deficient to meet criteria beyond high remnant polarization, including low leakage current levels, high stability and durability. However, the challenge of achieving ferroelectricity enhancement with reliability at back-end-of-line compatibility, which requires less than 400°C remains. [1], [2] Here, we demonstrate a ZrO_2-seed layer embedded ferroelectric $Hf_{1-x}Zr_xO_2$ films to control the phase ratios of tetragonal, orthorhombic, and monoclinic at low temperatures (<400°C). The ZrO_2-seed layer affects the initial growth with small grain nuclei of $Hf_{1-x}Zr_xO_2$ films which can manifest the ferroelectric transition. As a result, the ZrO_2-seed layer not only reduces the post-metallization annealing temperature but also achieves high remnant polarization with endurance exceeding 10^9 cycles. We also present that the different thickness of ZrO_2-seed layer affects ferroelectric properties. Specifically, ZrO_2-seed layer (5 cycles) embedded $Hf_{1-x}Zr_xO_2$ exhibits 30.3 μC/cm² of the remnant polarization value at 350 °C, respectively. These values showed better than those of $Hf_{1-x}Zr_xO_2$ films without (12.1 μC/cm²) and with 7 cycles of ZrO_2-seed layer (13.0 μC/cm²). It could be attributed to the different ratios between the non-ferroelectric tetragonal phase and the ferroelectric orthorhombic phase related to the ZrO_2-seed layer induced phase transition during the post-metallization annealing. Our finding suggests that atomic-level control of the ZSL is crucial for enhancing ferroelectricity while lowering the post-metallization annealing temperature. This indicates that optimizing the ZrO_2-seed layer is essential for high-performance ferroelectric $Hf_{1-x}Zr_xO_2$, enabling it to be compatible with back-end-of-line integration for future non-volatile memory architecture.

Acknowledgments

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AA-TuP-21 Highly Conductive Transparent Hybrid Superlattices with Excellent Gas-Barrier Properties and Flexibility, *Myung Mo Sung,* Hanyang University, Korea*;* ***Quang Khanh Nguyen****,* Hanyang University, Korea, Viet Nam

Transparent electrodes and passivation layers find extensive application in optoelectronic devices such as light-emitting diodes, solar cell. Integrating transparent conductive and gas diffusion barrier layers into a unified component holds promise for enhancing device performance and cost-effectiveness. In this study, we present a novel transparent conductive gas diffusion barrier achieved through a cutting-edge hybrid superlattice structure, combining ZnO with self-assembled monolayers. Fabricated using low-temperature atomic layer deposition and molecular layer deposition techniques, the superlattice demonstrated exceptional electric conductivity, attributed to the precisely designed phase-composite ZnO nanolayers. We systematically optimized the ZnO nanolayer thickness to attain a well-defined amorphous/crystalline phase-composite structure. The resulting superlattice, with a thickness of 100 nm, exhibited a low sheet resistance of 65 Ω sq^{-1} and maintained over 90% transmittance at a wavelength of 550 nm. The organic layers within the superlattice structure contribute to resilience against environmental degradation and mechanical deformation, achieved through the formation of a multilayered structure that effectively decoupled defects in the underlying layers. The hybrid superlattice exhibited robust electric conductivity, surpassing 1400 S cm^{-1} even after 15 days in damp heat conditions and exceptional moisture barrier characteristics (water vapor transmission rate < 4 × 10^{-7} g m^{-2} day^{-1}) alongside remarkable flexibility that retained the performance after 10,000 bending cycles. These compelling features position the hybrid superlattice as a promising candidate for transparent conductive gas diffusion barriers, with diverse applications in emerging optoelectronics.

AA-TuP-22 Enhanced Growth Stability of ZrO_2, HfO_2, and In_2O_3 Deposited by Liquid Injection Atomic Layer Deposition, *Il-Kwon Oh,* ***Soon-Kyeong Park****, Ji-Won Jang,* Ajou University, Republic of Korea

In conventional thermal atomic layer deposition (ALD), when a high number of ALD cycles is conducted, the vapor pressure of the precursor consumed often exceeds that generated, leading to a critical issue where the thickness of the deposited film decreases. This issue negatively impacts targeting the desired thickness of the thin film at high ALD cycles. Liquid injection atomic layer depositionvia a liquid deliverysystem (LDS) is an ideal thin-film deposition method for addressing this issue. Utilizing LDS ensures a consistent vapor pressure ratio of precursor during the process [1]. The LDS can handle most solid and liquid compounds including low vapor pressure, thermally labile, and viscous ones for the synthesis by ALD of thin films [2]. The LDS employment for the synthesis by metal-organic chemical vapor deposition (MOCVD) and ALD has been reported for vanadium oxide, and titanium oxide thin films [3-4]. Despite these advantages, research on thin films deposited via liquid injection atomic layer deposition is still few.

In this study, the excellent growth stability of ZrO_2, HfO_2, and In_2O_3, which are commonly used as gate dielectrics and channel materials, was confirmed through liquid injection atomic layer deposition, and the growth characteristics of these materials at high ALD cycles were specifically investigated. Cyclopentadienyl Tris(dimethylamino) Zirconium (Cp-Zr), Cyclopentadienyl Tris (dimethylamino) Hafnium (Cp-Hf), and (3-Dimethylaminopropyl) dimethyl indium (DADI) were used as the precursors, and O_3, H_2O as the oxygen source, to deposit on Si substratesSpectroscopic ellipsometry measurements were conducted to confirm the thickness of thin films deposited at various ALD cycles. X-ray photoelectron spectroscopy (XPS), which allows for the analysis of chemical composition ratios, was used to determine whether stable vapor pressure was maintained to form the thin film even at high ALD cycles. Consequently, this study is expected to provide insights into achieving stable thin film growth and precise thickness control for high ALD cycle applications through liquid injection atomic layer deposition.

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AA-TuP-23 Enhanced Cryogenic Stability and Endurance of CMOS-Compatible ALD $HfZrO_2$ FeCAPs with Optimized WO Interfacial Layer, ***Eunjin Kim****, Jiyong Woo,* Kyungpook National University, Republic of Korea

$HfZrO_2$-based ferroelectric capacitors (FeCAPs) are gaining attention as promising candidates for non-volatile memory devices due to their CMOS compatibility and ability to achieve low aspect ratios. Despite these advantages, a major challenge arises during the post-metallization annealing (PMA) process, which is crucial for realizing ferroelectricity. These

FeCAPs, typically fabricated on W-plugs, are prone to the unintended formation of a non-stoichiometric WO_x layer at HZO-electrode interface. This unwanted oxide layer induces defect states and increases oxygen vacancy (V_O) concentrations through a scavenging effect. To address this, we introduced sputtered amorphous WO interfacial layer(IL) engineering. The polarization-voltage (P-V) measurements showed remnant polarization (P_r) greater than 20 μC/cm^2 in the ALD-grown HZO FeCAP. However, the achieved polarization was vulnerable to PMA times, exhibiting leaky P-V curve explained by uncontrollable defects due to interfacial WO_x near the bottom electrode (BE). The introduction of 10 nm WO IL into the HZO FeCAP not only increased $2P_r$ to 52 μC/cm^2, but also enhanced the thermal stability of achieved P_r. Since a less prominent top interfacial layer was observed in the Transmission Electron Microscopy image, a sandwich-type WO/HZO/WO was also fabricated, but P_r was rather degraded. Next, the impact of WO IL stoichiometry was investigated by varying Ar/O_2 gas ratio during WO IL deposition. Unlike HZO FeCAP, where P_r was degraded noticeably with decreasing temperature, insertion of WO IL made P_r immune to temperature. Note that $2P_r$ greater than 58 (or 40) μC/cm^2 at 300 (or 123) K was achieved for the HZO/$WO_{2.8}$ FeCAP. The endurance characteristic proportional to the stoichiometry of WO IL. The relatively large amount of V_Os in the $WO_{2.4}$ IL can be easily clustered to form leakage paths, causing breakdown failure after 10^4 cycles. In contrast, leveraging more stoichiometric WO ILs (e.g., $WO_{2.8}$ or WO_3) can alleviate the interfacial or bulk defects that cause dipole pinning in the HZO, thereby improving endurance over 10^8 cycles. However, when stoichiometric WO_3 IL was used, P-V curve with increased coercive voltage began to be measured only at slow frequencies. This means that the applied voltage is less effectively used to rotate the dipoles in the HZO/WO_3 FeCAP. Therefore, introducing $WO_{2.8}$ IL enables an environment, where the intrinsic HZO properties can be robustly resilient to the interface defects by mitigating W BE scavenging effect. This resulted in larger diffraction intensity of the orthorhombic-phase in the HZO/$WO_{2.8}$, allowing most of the formed dipoles in the HZO to participate in switching.

AA-TuP-24 Thermal Atomic Layer Deposition of Ru-incorporated Molybdenum Carbide Thin Films via Inter-ligand Reaction for Advanced Copper Metallization, *Jeong Hwan Han,* ***Ji Sang Ahn****,* Seoul National University of Science and Technology, Republic of Korea

As the width of metallization wire in semiconductor device decreases, there is an increase in the overall resistance of Cu interconnect including diffusion barrier and seed layer. This not only limits the device speed but also hinders further scaling down of the device. Therefore, there has been growing demands for the development of materials that can serve as both the Cu diffusion barrier and seed layer. In this regard, atomic layer deposition (ALD) is an essential technique due to its ability to precisely control thickness down to the sub-nm level and excellent step coverage in complex structure. For decades, transition metal nitride and carbide multi-layer such as Ti/TiN, Ta/TaN, Ta/TaCN are widely introduced as Cu diffusion barrier and liner. Molybdenum-based carbide and nitride materials have recently gained attention as promising options for diffusion barrier and liner due to their high melting point, low resistivity, excellent thermal stability, and low reactivity with Cu.

In this study, Ru-incorporated MoC_x thin films were deposited from metal-organic Mo and Ru precursors by thermal ALD using inter-ligand reaction. Herein, Ru precursor was served as the counter-reactant for the Mo precursor without the use of common ALD reactant gases such as H_2 and O_2. The crystallinity, chemical binding states, impurity, and electrical characteristics of Ru-incorporated MoC_x were investigated. Additionally, atom probe tomography (APT) analysis confirmed the incorporation of Ru into the MoC_x matrix. The Cu diffusion barrier performance of ALD Ru-incorporated MoC_x was evaluated by fabricating Cu/Ru-incorporated MoC_x/Si structure, which was subsequently annealed at the high-temperatures for 15 min. The seed layer performance was also evaluated by carrying out Cu electroplating deposition depending on the thickness of the Ru-incorporated MoC_x films. In conclusion, Ru-incorporated MoC_x deposited by ALD can be considered a promising option for combined Cu diffusion barrier and seed layer applications.

AA-TuP-25 Stabilization of Metastable Rutile TiO_2 Through Engineering of the Upper Layer for Memory Applications, ***Jeon Ji Hoon****, Kim Seong Keun,* Korea Institute of Science and Technology (KIST), Republic of Korea

The increasing demand for DRAM memory density necessitates continuous scaling down of device size. The reduction in capacitor size compromises charge storage, leading to uncertainties in data read operations. To address this, materials with a higher dielectric constant than the currently used HfO_2 and ZrO_2 (~40) are needed. Rutile TiO_2, with a dielectric constant of 80–170 depending on crystallographic orientation, is a promising alternative. However, its metastable nature and high formation temperature pose challenges for integration.

A common approach to stabilizing rutile TiO_2 in the as-grown state via ALD is to use bottom electrodes such as RuO_2, IrO_2, SnO_2, and MoO_2, which provide lattice matching. However, this approach requires replacing existing bottom electrodes, complicating integration with current DRAM architectures. TiN, the industry-standard bottom electrode, does not have lattice matching with rutile TiO_2, making it difficult to apply these conventional methods.

In this work, we address the challenge of forming rutile TiO_2 in environments without lattice matching. Instead of relying on lattice-matched bottom electrodes, we induce rutile TiO_2 crystallization by introducing an upper layer with a rutile crystal structure. This approach enables the integration of high-k rutile TiO_2 while maintaining the TiN bottom electrode, ensuring compatibility with existing DRAM fabrication processes. Additionally, we discuss potential challenges associated with this method in the context of DRAM capacitors.

AA-TuP-26 Enhancing Plasma Resistance in Semiconductor Equipment with Atomic Layer Deposition Thin Films, *Young Yeon Ji,* ***Bongjun Koo****, Changsup Kwon, In-rae Park,* Hansol IONES, Republic of Korea

This study applies ALD coating to enhance plasma resistance and physical properties of semiconductor equipment chamber components in the corrosive environment of semiconductor processes. High-density plasma or corrosive gas can cause surface corrosion and contaminant particles to accumulate in the components, which can adversely affect semiconductor processes. To address this issue, ceramic material coatings are being applied to protect semiconductor equipment chamber components. Ceramic materials with excellent plasma resistance properties can be coated using various coating methods such as PVD (Physical Vapor Deposition), APS (Atmospheric Plasma Spray), AD (Aerosol Deposition), and ALD (Atomic Layer Deposition). Especially, ALD coating offers high resistance to plasma environments, superior step coverage, and conformity compared to other coating methods, enabling high-density uniform deposition even in complex 3D structures, making it a promising next-generation coating technology for semiconductor equipment chamber components. In this study, ALD coating was applied through the chemical reaction of yttrium, aluminum precursors along with oxidants such as water, O2, and O3 to produce yttrium oxide (Y2O3), aluminum oxide (Al2O3), and yttrium aluminum garnet (YAG) thin films with excellent plasma resistance properties. The physical properties and impurities in the deposited coating layer were analyzed using XPS, XRD, nano-indentation and SEM. These coating layers were applied to substrates made from various materials including metal, ceramic, polymer and complex 3D structures. This result is expected to enhance the reliability and performance of the semiconductor equipment chamber components.

AA-TuP-27 Crystallization Annealing-Free Ferroelectric Tunnel Junctions with ZrO_2 Seed-layer and HfO_2-ZrO_2 Superlattice, ***Kwang Min Jeong****, You Seung Rim,* Department of Semiconductor Systems Engineering and Convergence Engineering for Intelligent Drone, Sejong University, Republic of Korea

Ferroelectric tunnel junction (FTJ) devices have recently been considered promising candidates for non-volatile memory due to their non-destructive readout, low power consumption, and fast operation speed. Additionally, their two-terminal structure enables high-density integration with a compact $4F^2$ cell size. [1] In FTJs, the spontaneous polarization of the ferroelectric layer can be switched by an applied electric field, resulting in electrical resistance modulation depending on the polarization orientation. This phenomenon, known as tunneling electroresistance (TER), arises from changes in the electrostatic potential profile across the ferroelectric layer.[2] In this work, we investigate the switching mechanism of an Al/supercycle engineered ferroelectric HfO_2-ZrO_2/ZrO_2-seed/n++Si FTJ structure under different rapid thermal process (RTP) temperature. The ZrO_2 seed layer influences the initial growth of the HZO films by promoting the formation of small grain nuclei, which are crucial for the ferroelectric phase transition at low temperature.[3] Furthermore, the application of a HfO_2-ZrO_2ferroelectric superlattice enhances ferroelectricity due to tensile stress induced by the mismatch in their coefficient of thermal expansion (CTE) during atomic layer deposition and RTP. [4] Here, we demonstrate an annealing-free FTJ device that exhibits ferroelectricity even without RTP. Our strategies for achieving low-temperature processing, along with a

supercycle-engineered ferroelectric layer, lead to an in-depth understanding of their operating mechanism and pave the way for the development of ferroelectric memory switching devices.

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AA-TuP-28 Synthesis and Characterization of $SrTiO_3$ Thin Films by Atomic Layer Deposition with $Sr(dmts)(hfac)_2$ and $(CpMe_5)Ti(OMe)_3$, ***Sangyeon Jeong****, Jaejun Lee, Woongkyu Lee,* Department of Materials Science and Engineering, Soongsil University, Republic of Korea

High-capacitance capacitors are essential for achieving the high integration of DRAM. To meet this demand, trench structures with high aspect ratios are employed, and atomic layer deposition (ALD) is utilized to ensure excellent step coverage and uniformity. Traditionally, capacitance has been enhanced by reducing the dielectric thickness, however, this approach leads to increased leakage current, necessitating the use of high-k materials. $SrTiO_3$ (STO) has been extensively studied as a next-generation dielectric material because of its high dielectric constant exceeding 100. However, the low bandgap of $SrTiO_3$ (3.1–3.2 eV) and issues such as crack formation induced by film shrinkage during annealing have led to increased leakage current, presenting significant challenges for its application. From the perspective of precursors, cyclopentadienyl (Cp)-based Sr precursors have been the most extensively studied due to their high thermal stability and sufficient reactivity. However, their excessive interaction with the surface results in the retention of carbon ions from the ligands in the thin film, leading to the formation of strontium carbonate. This poses critical issues in impeding high quality perovskite $SrTiO_3$ phase formation.

In this study, we developed an ALD process for $SrTiO_3$ thin films using a novel Sr precursor, $Sr(dmts)(hfac)_2$, developed by the Korea Research Institute of Chemical Technology. To address the issue of $SrCO_3$ formation during SrO deposition, thermodynamically stable SrF_2 was deposited using $Sr(dmts)(hfac)_2$ and H_2O, while TiO_2 was deposited using $(CpMe_5)Ti(OMe)_3$ and O_3. The subcycle ratio of SrF_2 to TiO_2 was optimized to achieve stoichiometric cation composition of Sr:Ti = 1:1. Finally, post-deposition annealing in an air ambient eliminated fluorine and reduced carbon contamination of SrF_2-TiO_2, enabling the formation of stable $SrTiO_3$ thin films. In this study, we present SEM, XPS, XRD, and other analyses demonstrating the effective removal of fluorine impurities and the successful formation of the perovskite crystalline structure in $SrTiO_3$. The $SrTiO_3$ thin films exhibited a high bulk dielectric constant exceeding 100 in planar-structured metal-insulator-metal capacitors, highlighting their potential as a next-generation dielectric material for DRAM capacitors.

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AA-TuP-29 Ozone Post-Treatment for Highly Stoichiometric TiO_2 Thin Films with Improved Dielectric Performance*,* ***Juan Hong****, Hyeongjun Kim, Woongkyu Lee,* Department of Materials Science and Engineering, Soongsil University, Republic of Korea

In the semiconductor industry, as DRAM and other memory devices continue to shrink, high-k dielectrics are crucial for maintaining capacitance and reducing leakage current. Atomic layer deposition (ALD) processes, which enable precise thickness control, excellent step coverage, and large-area uniformity of thin films, has been essential for the deposition of high-k materials. TiO_2, a high-k material, has gained significant attention as a next-generation dielectric material due to its high permittivity, ranging from 40 to 80 depending on its crystalline phase. However, its narrow bandgap of 3.2–3.35 eV and n-type property due to the oxygen vacancies, lead to high charge mobility and leakage current. The presence of oxygen vacancies also causes deviations in the Ti:O ratio from its stoichiometric composition, resulting in crystalline distortions. A certain portion of other phases such as Ti_2O_3 and Ti_4O_7, in the films decreases the crystallinity of TiO_2 and consequently reduces the dielectric constant of the films.

In this study, ozone post-treatment was applied to TiO_2-based planar capacitor fabrication to improve the stoichiometry and crystallinity of TiO_2 thin films by inducing oxygen diffusion. TiO_2 thin films were deposited via ALD at 250 °C using trimethoxy(pentamethylcyclopentadienyl)titanium as the Ti-precursor and ozone (200 g/m^3) as the reactant. After TiO_2 deposition, ozone post-treatment was performed at 250 °C by injecting ozone (200 g/m^3) for 5, 10, 15 and 20 minutes. The Pt top electrode was deposited via sputtering to fabricate planar capacitors with the structure Pt (60 nm)/TiO_2 (20 nm)/TiN (100 nm). By various surface characterization, it was revealed that ozone post-treatment enhanced the crystallinity of the anatase phase. Regardless of the treatment duration, the refractive index and film density of the TiO_2 thin film approached theoretical values compared to the as-deposited film, which exhibited a refractive index of 2.23 and a density of 3.33 g/cm^3. Additionally, the effect of ozone post-treatment on the electrical properties and polarization mechanisms was investigated. The as-deposited TiO_2 film exhibited a dielectric constant of 42, which increased by 29% after 15 minutes of ozone post-treatment, reaching 54 even in the anatase phase. Concurrently, the impact of ozone treatment on leakage current degradation was negligible.

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AA-TuP-30 Mobility Enhancement in In_2O_3/Al_2O_3 Nanolaminate Structures Grown by Atomic Layer Deposition*,* ***Kyunghun Lyu****, Woongkyu Lee,* Department of Materials Science and Engineering, Soongsil University, Republic of Korea

As device integration advances, capacitors and transistors are becoming smaller, thin films are getting thinner, and device structures are evolving from planar to three-dimensional designs. However, A major limitation of silicon single-crystal substrates, currently used as channel materials, is their difficulty in being applied to 3D structures. In contrast, oxide semiconductors, which can be deposited by physical/chemical vacuum processes, are gaining attention as next-generation channel materials. Among various deposition methods, atomic layer deposition (ALD) is particularly advantageous due to its self-saturating growth behavior, which allows precise control of thickness at the atomic layer level and providing high step coverage even in complex 3D structures. Nevertheless, ALD also faces challenges in achieving compositional uniformity of multi-component materials such as indium gallium zinc oxide which is one of the most promising oxide semiconductors. Therefore, employing the two-dimensional electron gas (2DEG) has gained increasing attention as a method to achieve high mobility through heterostructures.

In this study, a nanolaminate structure was fabricated by alternately stacking semiconducting In_2O_3 (IO) layer and insulating Al_2O_3 (AO) layer. IO and AO thin films were deposited through an ALD process at 300°C with (3-Dimethylaminopropyl)dimethylindium (DADI) and trimethylaluminum (TMA)as In and Al precursors, respectively. High density (~200 g/m^3) O_3 and H_2O were used as an oxygen source for each ALD process. To investigate the conducting characteristics of the nanolaminate structure, various configurations were fabricated. By Hall effect measurement, no mobility change was observed with varying IO thickness, however mobility obviously increased by 77.5% from 22.2 cm^2/Vs for In_2O_3 single layer to 39.4 cm^2/Vs for a stack of only AO/IO/AO/IO/AO structure. Through variations in AO thickness, it was confirmed that the 2 nm AO/5 nm IO stacked structure exhibited the highest mobility of 48.6 cm^2/Vs which was 117.9% higher than 10 nm IO single layer. For further investigation, ARXPS measurements were conducted at various angles, revealing a significant presence of oxygen vacancies at the interface. Additionally, VBO calculations were performed to evaluate the electronic band alignment and interpret the mobility enhancement observed in the nanolaminate structures.

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AA-TuP-31 Evaluation of Molybdenum Oxidation for the Growth of Rutile TiO_2, *Jin Tae Noh,* ***Kyong Min Kim****, Byeong Hyeon Kang, Seokjun Han, Seok Nam Koh, Tae Wan Lee,* Wonik IPS, Republic of Korea

Molybdenum dioxide (MoO_2) has attracted attention as a next generation electrode material in DRAM devices. It has been exhibited low leakage current property in MoO_2/TiO_2 based MIM capacitor structure because MoO_2 has a high work function. Also, when TiO_2 deposited on the MoO_2

film, it has been reported that the TiO_2 film tends to form rutile structure. The high capacitance property has been demonstrated in the rutile phase of TiO_2. But, despite these advantages of MoO_2, there are significant challenges in achieving the molybdenum oxide with a proper stoichiometry. In the previous studies, these MoO_x films must be conducted by an additional reduction process for the formation of MoO_2 after the molybdenum oxide (MoOx, 2<x<3) was deposited.

In this study, the oxidation process as a new approach method has been evaluated for the formation of MoO_2 using a molybdenum metal layer. First, the molybdenum metal layer was deposited using MoO_2Cl_2 and H_2 by ALD methods, and then, the oxidation process was carried out at different temperatures using oxygen and ozone as an oxidizer, respectively. In conclusion, MoO2 films were successfully formed through the oxidation of molybdenum using ozone. These films were analyzed using techniques such as X-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM). Additionally, prior to the oxidation process, the very thin TiO_2 capping layer was deposited on the molybdenum to enhance surface morphology and to improve MoO_2/TiO_2 interface properties. Finally, a TiO_2 layer was deposited as a capacitor layer using ALD method. The above processes carried out in-situ successfully result in rutile TiO_2 crystallinity within the MoO_2/TiO_2 multilayer. This molybdenum oxidation process shows promise for applications of MoO_2/TiO_2 based DRAM devices.

AA-TuP-32 Fast, Remote Plasma ALD of Highly Conductive TiN for Quantum Applications, ***Arpita Saha***, *Dmytro Besprozvannyy, Yi Shu, Agnieszka Kurek,* Oxford Instruments Plasma Technology, UK*; Harm Knoops,* Oxford Instruments Plasma Technology, UK, Eindhoven University of Technology, UK

Quantum devices rely on precise control of coatings and material properties at the atomic scale for high performance. Through-Silicon vias are a critical enabler for the next generation of quantum technologies as they provide high-density interconnects, reduced signal loss and improved scalability. Plasma Enhanced ALD (PEALD) is known for its unmatched precision, tuneability and ability to deposit high-quality uniform thin films over large area substrates making it indispensable in production of materials for quantum applications. TiN has gained attention especially for development of superconducting resonators due to its tuneable superconducting properties, chemical stability and compatibility with scalable fabrication methods. Achieving pristine quality superconducting nitrides using ALD can be extremely challenging due to low growth-rates, long cycle times or due to incorporation of background impurities.

In this contribution we will show PEALD results from Oxford Instruments Plasma Technology's recently launched ALD platform, PlasmaPro ASP (PPASP) system aimed towards R&D customers. The remote Capacitively Coupled Plasma (CCP) source and chamber design allows efficient surface reactions for better film quality at a faster rate with low plasma damage. PPASP can deliver different superconducting nitrides along with different variants of TiN using either halide or metal organic chemistry for targeted quantum applications. We have been able to demonstrate deposition of smooth TiN films (roughness below 500 pcm) ranging from 5nm to 200nm using PPASP at high throughput ($\geq$50 nm/h) using metal organic chemistry at low temperatures of 275 ˚C, with room temperature planar resistivity <200 μΩ.cm and good superconducting properties with T_c > 1K. However, these films show slightly larger C (~6 at%) content along with poor via resistivity. To expand the TiN capabilities further, we have developed the halide-based TiN recently using both H_2/N_2 and NH_3 plasma. Tuning the N_2/H_2 ratio in the plasma mix translates direct tuneability of the resistivity and growth per cycle (GPC). NH_3 enhances the GPC, while the H_2/N_2 plasma helps in achieving very low resistivity values of <50 μΩ.cm. The films are polycrystalline and can achieve $\geq$ 85% conformality as confirmed by XRD and SEM. XPS and ToF-SIMS depict minimal O (<3 at%) and negligible C (<0.2 at%) and halide impurity (<0.2 at%) levels while roughness is ~1.5 nm. These films can achieve better via resistivity and stress tuneability for thicker films using recipe parameters. The tuneability of the TiN deposition process using PPASP makes it a promising candidate to tackle material challenges in quantum applications.

AA-TuP-33 Optimized Interface Engineering of ALD SrTiO3 for DRAM Capacitors, *Seong Keun Kim,* ***Seung Wan Ye***, *Hong Keun Chung, Jeon Jihoon,* Korea Institute of Science and Technology (KIST), Republic of Korea

Strontium titanate ($SrTiO_3$, STO) has been extensively studied as a next-generation dielectric material for DRAM capacitors due to its exceptionally high dielectric constant. However, its direct integration with ruthenium (Ru) bottom electrodes presents significant interfacial challenges that hinder its practical application. One of the most critical issues is the compositional inhomogeneity induced by excessive initial SrO growth at the STO/Ru interface. Consequently, STO films grown on Ru remain amorphous or require post-deposition annealing (PDA) at temperatures exceeding 600°C to achieve crystallization, which is incompatible with DRAM manufacturing constraints.

To mitigate interfacial reactions at the STO-Ru interface, we investigated multiple techniques to suppress SrO overgrowth. One effective approach was the insertion of an ultra-thin Pt interlayer (<1 nm) on Ru, which successfully induced in-situ crystallization during ALD. This method facilitated the formation of a high-quality perovskite structure, resulting in a significantly enhanced dielectric constant and an equivalent oxide thickness (EOT).

To further improve STO's electrical performance, we explored perovskite-based bottom electrodes that provide better lattice matching with STO. By evaluating STO growth on these alternative electrodes, we assessed their potential to enhance dielectric properties and ensure scalability for next-generation DRAM capacitors.

AA-TuP-34 Urea Production from Polluted Seawater by Atomic Layer Deposited Catalytic Layers, ***Rens Kamphorst***, *Peter M. Piechulla, Ruud J. van Ommen,* Delft University of Technology, Netherlands

Soil and water pollution, in particular driven by agricultural activity, has become a major concern over the last decade. Dissolved nitrates, introduced in water systems by excess fertilizer, disrupt ecosystems and potentially affect marine environments. Effective ways to remove these pollutants from waterways are limited, and expensive.

Within the Horizon Europe project ICONIC, we aim to address this issue by developing systems that electrochemically convert these contaminants, along with dissolved CO_2 into urea, thereby closing the nitrate cycle while providing a sustainable source of fertilizer. A key challenge within the project is the design of catalytic layers to facilitate the simultaneous conversion of nitrates and carbonates into urea. Prior literature identified copper-zinc as a promising candidate material to be used for these layers[1]. Here, ALD stands out as a tool to achieve a unique level of uniformity of the catalyst layer as well as the chemical composition of the copper-zinc compound catalyst. An additional challenge in the context of the application of the layers is maintaining the catalytic performance in the presence of seawater. In this environment, high salinity and dissolved species likely lead to corrosion and fouling of the catalytic layer. To mitigate this, we propose a protective SiO_2 overcoat, demonstrated in a prior study to extend the operational lifetime of electrocatalysts without compromising their activity[2].

Our poster will outline the conceptual framework of our approach, discuss early-stage experimental progress, and highlight the broader potential of this technology for environmental remediation and agricultural sustainability.

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[2] Li et al., *Catal. Sci. Technol.* **14**, 1328-1335 (2024) ,10.1039/D3CY00996C

AA-TuP-35 Tailoring the Scavenging Effect of ALD-Al_2O_3 Passivation Layer via Oxidant Engineering for High-Performance Tellurium Transistors, ***Jaeyoon Shim***, *Jaemin Jung, In-Hwan Baek,* Inha University, Korea (Democratic People's Republic of)

As the two-dimensional (2D) downscaling of silicon-based semiconductors approaches fundamental physical limits, Monolithic 3D (M3D) integration has emerged as a promising alternative to overcome these challenges. However, realizing high-performance p-type transistors for M3D CMOS integration remains challenging due to the limited hole transport characteristics of conventional oxide semiconductors and the constraint of a low thermal budget (<400°C). Recently, Tellurium (Te) has garnered attention as a next-generation BEOL-compatible p-type material due to its high hole mobility and low-temperature processability, but its rapid and uncontrollable crystallization at room temperature and the formation of an amorphous native oxide degrade device stability and performance. Therefore, an effective passivation strategy is required to enhance the reliability of Te-based thin-film transistors (TFTs). Atomic layer deposition (ALD) is a suitable technique for forming high-quality passivation layers due to its precise thickness control and excellent uniformity. Al_2O_3, with a lower formation energy than tellurium oxide, has been reported to reduce trap density and scavenge the native amorphous tellurium oxide, thereby improving crystallinity. The choice of oxidant in ALD significantly influences the passivation layer quality by affecting the scavenging behavior, chemical

composition, and impurity incorporation. Therefore, optimizing the oxidant selection is critical for achieving stable and high-performance Te-based TFTs. In this study, we fabricated Te TFTs and applied ALD passivation using Al_2O_3 with various oxidants (O_3, H_2O, and H_2O_2). By analyzing the electrical performance of the TFTs, we demonstrated that oxidant selection plays a crucial role in modulating the scavenging effect on Te channel layer, thereby impacting trap states, chemical composition, and overall device performance. This study contributes to expanding the selection of ALD oxidants for Te TFT passivation, providing an optimized strategy for high-performance and stable p-type TFTs.

AA-TuP-36 Selective Surface Passivation for Ultrathin and Continuous Metallic Films via Atomic Layer Deposition, *Seong Keun Kim,* KU-KIST Graduate School of Converging Science & Technology, Korea University, Republic of Korea*; Han Kim, Taeseok Kim,* ***Minseok Kim****, Jihoon Jeon, Gwang Min Park,* KU-KIST Graduate School of Converging Science and Technology, Korea University, Republic of Korea*; Sung-Chul Kim, Sung Ok Won,* Korea Institute of Science and Technology (KIST), Republic of Korea*; Ryosuke Harada,* TANAKA, Japan*; Sangtae Kim,* Department of Nuclear Engineering, Hanyang University, Republic of Korea

Scaling demands in modern electronics increasingly require ultrathin metallic films (<3–4 nm) that maintain high continuity and low surface roughness. However, the inherently high surface energy of metals on dielectric substrates (e.g., Al_2O_3, SiO_2) often promotes island-like growth, making the formation of uniform, continuous ultrathin layers exceedingly difficult. Here, we present a novel strategy to substantially reduce the disparity in adsorption behavior between metallic and dielectric surfaces, thereby enabling the realization of continuous films at significantly lower thickness.

Our approach employs aniline as a small-molecule inhibitor that preferentially adsorbs on existing metallic nuclei rather than on dielectric regions. By introducing an additional inhibitor-injection step prior to dosing the metal precursor, lateral growth on metal surfaces is effectively suppressed, while nucleation on adjacent dielectric areas is enhanced. Following precursor adsorption, an oxidizing agent (O_3) completes the metal-oxide reaction and removes the inhibitor, restoring surface reactivity for subsequent cycles. Repetitive application of this process significantly increases nucleation density and drastically reduces the film thickness required for achieving continuity.

Using this inhibitor-modified ALD protocol, we demonstrate continuous Ir films at thicknesses as low as ~1 nm and Pt films at ~2.3 nm. Compared to conventional ALD, these ultrathin layers exhibit improved surface smoothness and reduced electrical resistivity. Notably, this approach is especially advantageous for metal precursors with long nucleation delays, indicating its broad versatility across different metal-precursor systems.

Overall, this selective surface-passivation ALD approach pushes the limits of ultrathin metal film deposition, delivering reliable solutions for advanced interconnects, high-density memory electrodes, and other next-generation components. By mitigating metal nucleation challenges on dielectric substrates, it further drives miniaturization and improves device performance in future semiconductor technologies.

AA-TuP-37 Atomic Layer Deposition-Enabled Lateral Conversion of Transition Metal Dichalcogenides for Electrochemical Hydrogen Generation, ***Asem Jakyp****,* Nazarbayev University, Kazakhstan*; Aidar Kemelbay,* Lawrence Berkeley National Laboratory*; Arman Tuigynbek, Alexander Tikhonov,* Nazarbayev University, Kazakhstan

Transition metal dichalcogenides (TMDs), a class of van der Waals materials, have gained significant attention for their potential in electronic, optoelectronic and catalytic applications due to their highly tunable electronic and optical properties. However, achieving wafer-scale, precisely controlled synthesis of TMDs remains a critical challenge for scalable device integration. In this work, we present lateral conversion, a novel synthesis approach that enables the fabrication of patterned TMD structures with precise thickness control at lithographically defined locations. The method is facilitated by atomic layer deposition (ALD), which ensures angstrom-level thickness precision, large-area uniformity, and versatility in selecting metal oxides for subsequent conversion into TMDs for catalytic applications. The lateral conversion process involves the chalcogenation of ALD-deposited metal-oxide films, sandwiched between silica layers. This configuration effectively protects the TMD basal plane from contamination and oxidation, while simultaneously exposing catalytically active edge sites — an essential feature for efficient electrocatalysis. We demonstrate the fabrication of lithographically defined WS_2, MoS_2 and their alloys using lateral conversion, with in-depth characterization via Raman spectroscopy, photoluminescence (PL) mapping, and scanning electron microscopy (SEM). The catalytic efficiency of the synthesized TMDs is evaluated using a three-electrode electrochemical setup to assess their performance in the hydrogen evolution reaction (HER). The ALD-enabled precise thickness and composition control, patterning capability, scalability, and catalytic performance of this approach establish lateral conversion as a promising platform for the large-scale synthesis of TMD-based electrocatalysts.

AA-TuP-38 Low-Temperature Thermal Atomic Layer Deposition of Gallium Nitride Thin Films, ***Jian Heo****, Yerim Choi, Hyeji Kim, Okhyeon Kim, Hye-Lee Kim, Won-Jun Lee,* Sejong University, Republic of Korea

Gallium nitride (GaN), a wide direct bandgap III-V semiconductor, is widely used in power electronics and optoelectronic devices, such as high electron mobility transistors (HEMTs) and light-emitting diodes (LEDs). GaN films are typically grown at high temperatures using metal-organic chemical vapor deposition (MOCVD). However, thermal atomic layer deposition (ALD) offers an alternative method for high-quality GaN growth at lower temperatures, making it suitable for deposition on temperature-sensitive substrates and devices while avoiding plasma-induced damage. Despite extensive research on the plasma-enhanced ALD (PEALD) of GaN, low-temperature thermal ALD of GaN remains largely unexplored. In this study, GaN films were deposited by thermal ALD at temperatures below 250°C, and their properties were systematically analyzed. Self-limiting growth was confirmed by alternating exposure to a Ga precursor and ammonia. At 200°C, the growth rate was 1.3 Å/cycle, and the refractive index was 2.13, which is close to that of polycrystalline GaN (2.19 [1]). In addition, the deposited GaN films exhibited a stoichiometric composition with minimal impurities. Step coverage, density, crystallinity, and optical bandgap were investigated at different deposition temperatures to evaluate the effect of deposition temperature on the film properties.

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AA-TuP-39 High-Performance p-Type SnO Thin Film Transistor with Raised Source/Drain using Dry Etching Method, ***Jaemin Jung****, Jaeyoon Shim, InHwan Baek,* InHa University, Korea (Democratic People's Republic of)

Tin monoxide (SnO) has emerged as a promising p-type oxide semiconductor for back-end-of-line (BEOL) complementary metal-oxide-semiconductor (CMOS) integration due to its high hole mobility, which originates from the hybridization of Sn 5s and O 2p orbitals in the valence band. [1] However, the formation of a Schottky barrier at the oxide semiconductor/metal interface results in high contact resistance at the source/drain (S/D) regions, limiting device performance. Increasing the channel thickness can be an effective approach to reducing contact resistance. However, it inevitably leads to trade-offs, including increased off-current and significant negative shift of threshold voltage (V_{th}), which ultimately degrades electrical performance. To address this issue, Si, Mengwei, et al. proposed a raised S/D structure for n-type ITO thin-film transistors (TFTs) using a recessed channel formed by wet etching.[2] However, its isotropic etching profile induces unintended channel undercut, which may degrade device performance. Moreover, the excessively high etch rate of wet etching is not suitable for precise nanometer-scale channel thickness control. In contrast, dry etching methods such as reactive ion etching (RIE) and atomic layer etching (ALE) enable precise etch-depth control due to their anisotropic etching profiles and superior nanoscale patterning capability, making them highly suitable for recessed channel formation. Therefore, optimizing dry etching processes is essential for fabricating high-performance p-type SnO TFTs with a raised S/D structure. In this work, we optimized the dry etching process for ALD-deposited SnO thin films using Cl-based gases by analyzing the surface roughness and chemical composition to refine the etching conditions. Also We fabricated SnO TFTs with a raised S/D structure and systematically evaluated the impact of recessed channel thickness on device electrical performance. Furthermore, we investigated the dependence of contact resistance on SnO film thickness and demonstrated high-performance SnO TFTs through optimized recessed channel engineering. This study presents a novel approach for atomic-scale processing of p-type SnO TFTs, paving the way for their application in BEOL CMOS integration.

[1] Zhang, Wei, et al. *Journal of Physics: Condensed Matter* 34.40 (2022): 404003

[2] Si, Mengwei, et al. *ACS nano* 14.9 (2020): 11542-11547.

AA-TuP-40 Gain Enhancement of Microchannel Plate Detectors via ALD Coatings Inside the Channels, *Sun Gil Kim, **Min Seop Song**, Hyun Mi Kim, Ki Hun Seong, Sung Kyu Jang, Jong Hyun Choi,* Korea Electronics Technology Institute (KETI), Republic of Korea*; Yu Bin Nam,* Kyonggi University, Republic of Korea*; Jeong Gil Na, Kyung Hwan Jeong,* JJ CNS, Republic of Korea*; Seul Gi Kim, Hyeong Keun Kim,* Korea Electronics Technology Institute (KETI), Republic of Korea

In semiconductor manufacturing equipment, time-of-flight mass spectrometry (ToF-MS) is widely employed for real-time process exhaust gas monitoring. This technique determines mass-to-charge ratio based on ion flight time, offering high sensitivity and rapid analysis capability. One of the essential components in ToF-MS, the Microchannel Plate (MCP), serves as an electron multiplication and signal amplification device, enabling efficient detection and amplification of ion signals.

Conventional MCPs are fabricated from lead glass, where a SiO_2 emissive layer is formed during glass fabrication, facilitating electron multiplication. However, despite materials such as MgO and Al_2O_3 exhibiting superior secondary electron emission (SEE) properties compared to SiO_2, conventional deposition techniques such as physical vapor deposition (PVD) and chemical vapor deposition (CVD) have limitations in achieving uniform coating inside MCP channels. In contrast, atomic layer deposition (ALD) technology enables precise and uniform coating of materials with excellent electron multiplication properties even within the narrow MCP channels, thereby enhancing MCP performance. In this study, we developed the ALD process to deposit Al_2O_3 as a resistive layer and MgO as an emissive layer inside MCP channels. Bis(ethylcyclopentadienyl)magnesium ($Mg(EtCp)_2$) was used as the precursor for MgO, TMA(Trimethylaluminum) ($Al(CH_3)_3$) for Al_2O_3, and Deionized water (H_2O) as the reactant.

Film thickness and density were analyzed using an ellipsometer and X-ray reflectometry (XRR). Additionally, X-ray photoelectron spectroscopy (XPS) was employed to examine the elemental composition and Mg/O ratio across different film thicknesses. The crystal structure was characterized using X-ray diffraction (XRD), while high-resolution transmission electron microscopy (HR-TEM) was utilized to investigate the microstructure of the deposited films. Moreover, the secondary electron emission (SEE) coefficient of MgO thin films under various process conditions was measured using a γ-focused ion beam (γ-FIB) system, and based on these results, the optimal process parameters and film thickness were determined.

This study is expected to serve as a key reference for material selection in emissive and resistive layers of MCP. Future research will explore various oxide thin-film combinations and novel materials, not only to enhance MCP gain but also to improve MCP lifetime and noise characteristics, thereby contributing to overall performance advancements. Moreover, the findings can be applied across various industrial and research fields, including time-of-flight mass spectrometry (ToF-MS) and image intensifiers.

AA-TuP-41 Effects of Alkali-Metal Doping on Aluminum-Silicate Coated Titanium Oxide Thin Film Transistors Prepared by Atomic Layer Deposition, ***Ryo Miyazawa**, Haruto Suzuki, Hibiki Takeda, Bashir Ahmmad Arima, Fumihiko Hirose,* Graduate School of Science and Engineering, Yamagata University, Japan

Thin-film transistors (TFTs) are used as pixel-control switching devices in displays. In this study, we developed surface-sensitive TFTs with 16 nm-thick titanium oxide channel for high mobility. The fabricated TFTs exhibited significant current amplification in the milliampere range with Na doping. We used aluminum-silicate films prepared by room temperature atomic layer deposition (RT-ALD) as the sodium adsorption layer. We reported the experimental results at the ALD/ALE conference 2024. It was reported that aluminum-silicate films exhibited adsorption abilities not only for Na but also for K and Cs. On the other hand, the Na-doped TFTs might be a contamination sources for other Si devices in LSI. Hence, in this study, we examined K and Cs doping instead of Na for the TFTs. In the conference, we will also discuss on the operation mechanism.

TiO_2 films were deposited on a Si substrate with a thermally grown SiO_2 layer by ALD. The TiO_2 thickness was set at 16 nm, with tetrakis(dimethylamino)titanium (TDMAT) as a Ti precursor. Plasma-excited humidified argon generated with an RF power of 500 W was employed as the oxidizing agent. The films underwent heat treatment at 500 °C for 30 minutes under the atmosphere for crystallization. Subsequently, Ti electrodes with a thickness of 100 nm were fabricated by electron-beam evaporation using a metal mask. For the gate electrode, the oxide film was selectively removed, followed by indium (In) deposition. Finally, a 10 nm-thick aluminum-silicate layer was formed as an alkali-metal adsorption layer via RT-ALD. Tris(dimethylamino)silane (TDMAS) and trimethylaluminum (TMA) were used as the precursors of Si and Al, respectively. The plasma power for oxidation during this process was 100 W. Figure 1 presents a schematic of the TiO_2-TFT with aluminum-silicate as the alkali metals adsorption layer.

Figure 2 shows the I-V characteristics of TiO_2-TFT after immersion in CsCl solutions. Even in the case of cesium doping, we confirmed current enhancement to the same milliampere level as with sodium. On the other hand, it was difficult to confirm the saturation region. We assume that the contact resistance limits the output currents [1]. In the conference, we discuss the effects of alkali metals on TiO_2-TFT.

AA-TuP-42 Influence of Atomic-layer-deposited MoNx Layers on Ferroelectric Properties of Hf-Zr-O Capacitors, *Jeong Hwan Han, **Jeong min Han**, Wangu Kang,* Seoul National University of Science and Technology, Republic of Korea

Ferroelectric (FE) materials have attracted significant attention for next-generation memory technologies, such as ferroelectric random-access memory (FeRAM), which offers advantages over flash memory, including higher speed and lower power consumption. Among various FE materials, HfO_2-based materials with a fluorite structure have been particularly notable due to their stable ferroelectricity even at sub-10 nm thicknesses, low leakage current resulting from a large bandgap (>5 eV), and excellent compatibility with CMOS technology. However, since HfO_2-based ferroelectrics are multi-phase materials containing both FE and non-FE phases, they tend to exhibit relatively low remnant polarization (2Pr) compared to conventional perovskite-based ferroelectrics, which limits their memory performance. Recent studies have focused on enhancing the 2Pr of $HfZrO_x$ (HZO) by methods such as doping, oxygen vacancy engineering, and in-plane tensile stress. Among these, oxygen vacancies have been shown to promote the crystallization and stabilization of the ferroelectric orthorhombic phase of HZO during rapid thermal annealing.

In this study, we investigate the enhancement of ferroelectric properties in HZO by introducing atomic-layer-deposited (ALD) MoN_x thin films. To evaluate the ferroelectric performance of HZO, metal-ferroelectric-metal (MFM) capacitors with a Pt/HZO/TiN structure were fabricated, and ALD MoN_x films were inserted at different locations (HZO/BE bottom interface, middle of HZO, and TE/HZO top interface). The impact of MoN_x films and their positioning on the ferroelectric properties and reliability of HZO was assessed. Through this investigation, we identified the optimal insertion condition for ALD MoN_x films to achieve superior ferroelectric performance in HZO.

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AA-TuP-43 Enhanced Stability of Ultrathin Mo-Passivated RuO2 Bottom Electrodes for TiO2-Based DRAM Capacitors, *Han Jeong Hwan, **Choi Seon Gu**, Lee Jae Hyeon,* Seoul National University of Science and Technology, Republic of Korea

As dynamic random access memory (DRAM) capacitors continue to scale down to enhance integration density, maintaining sufficient capacitance for reliable operation has become increasingly difficult due to structural constraints. This challenge necessitates the development of new high-k dielectric materials. Among potential candidates for metal-insulator-metal (MIM) capacitors, rutile TiO_2 stands out with a high dielectric constant of 70–170 and the ability to grow epitaxially on a bottom electrode with a matching rutile structure. Consequently, the advancement of compatible electrode materials is crucial for integrating these new dielectrics. Ruthenium oxide (RuO_2) is a promising metal oxide electrode for TiO_2-based MIM capacitors due to its rutile structure, low resistivity (~35 μΩ·cm), and high work function (~5.1 eV). However, during the atomic layer deposition (ALD) of TiO_2 on RuO_2 electrode, exposure to the Ti precursor and O_3 oxidant caused repeated reduction and etching of the RuO_2 surface, resulting in degradation of its morphology, structure, and electrical properties.

To address this issue, this study introduces an ultrathin Mo-passivated RuO_2 (Mo/RuO_2) bottom electrode to mitigate RuO_2 surface degradation during the ALD TiO_2 process. The crystalline structure and surface morphology were characterized using grazing incidence X-ray diffraction (GAXRD) and atomic force microscopy (AFM). TiO_2-based MIM capacitors were fabricated on the Mo/RuO_2 electrode, and X-ray fluorescence (XRF) and Auger

electron spectroscopy (AES) analyses were conducted to evaluate the initial TiO_2 growth behavior and compositional variations. These analyses confirmed that the Mo interlayer effectively suppressed the reduction and etching of RuO_2. The ultrathin Mo layer facilitated the epitaxial growth of rutile TiO_2, improved interfacial and dielectric properties of ALD TiO_2, and significantly improved the device reliability.

Acknowledgements

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AA-TuP-44 Towards Ultra-Low Resistivity of Titanium Nitride PEALD Layers Grown on an Amorphous SiO_2 Substrate with Aluminum Nitride Interfacial Layer, ***Valentina Korchnoy***, Technion Israel Institute of Technology, Israel; *Inna Popov,* The Hebrew University of Jerusalem, Israel; *Yael Etinger,* Technion Israel Institute of Technology, Israel; *Michael Lisiansky,* Tower Semiconductors, Israel

TiN layer is an important electrode material for modern electronic devices due to its low resistivity, scalability, and compatibility with CMOS technology. The plasma Enhanced Atomic Layer Deposition (PEALD) technique is widely used for growing uniform and conformal thin layers of TiN. The resistivity of thin TiN PEALD film is strongly influenced by the underlying substrate. Thin TiN layer of ultra-low resistivity (~ 10.5 μΩ.cm) has been achieved by PEALD on a sapphire substrate with AlN interfacial layer (IL) [1]. This resistivity is close to the bulk value. Such a low resistivity of the 14 nm TiN film can be attributed to its quasi-epitaxial manner of growth on AlN IL and low defect density of the layer. The perfect lattice matching between the (0001) sapphire substrate, AlN IL, and TiN is a dominant factor in the TiN layer performance. The AlN IL as thin, as 8 nm, is enough to grow a well-textured quasi-epitaxial TiN film. However, in TiN grown on an amorphous substrate (SiO_2) with AlN IL of the same thickness, the quality of the TiN layer is significantly worse, because TiN turned out to be poorly textured. As a result, its resistivity becomes approximately an order of magnitude higher than that of TiN grown on a sapphire substrate with the same thickness of AlN IL. This result was attributed to the poor structural performance of the AlN seed layer grown on an amorphous substrate (small polycrystal size without clear texturing).

The atomic layer annealing (ALA) technique used for the deposition of AlN layer supplies additional energy to stimulate surface reactions, increase the metal adatoms mobility and densification of the deposited film. Another factor that can improve the AlN IL quality is the layer thickness. As shown in [2], an increase in the thickness of the AlN layer leads to enhancement of its crystallinity.

The goal of our study is to determine the critical AlN IL thickness that provides a well-textured “seed” layer for subsequent deposition of ultra-low resistivity TiN films for electronic device applications. We suppose that the performance of on-grown TiN film will be close to those obtained on a sapphire substrate.

The AlN layers of 12 and 66 nm thickness were deposited by PEALD, using N_2/Ar plasma on 100 Å thermal oxide layers grown on a Si (001) substrate. The layers were characterized by XRD, XRR, TEM and spectroscopic ellipsometry. Structural analysis of the layers shows that PEALD AlN IL with a thickness of ~60 nm grown on amorphous SiO_2 substrate provides a well-structured template for the subsequent deposition of quality TiN films with low resistivity.

AA-TuP-45 High-Performance Tio2 Hardmask for sub-10 Nm Advanced Memory Patterning, ***Heongyu Lee***, *Seul-Gi Kim, Cheongha Kim, sumin Lee, Hyun-mi Kim, Sun Gil Kim, Jong Hyun Choi, Hyeongkeun Kim,* Korea Electronics Technology Institute (KETI), Republic of Korea

Si-based spin-on-hardmask (SOH) has been widely used in semiconductor processes; however, as the half-pitch approaches 10 nm, issues related to the deterioration of final wafer patterning quality arise due to deformation caused by the insufficient elastic modulus during etching or cleaning processes. To address this issue, new hardmask materials, including Ti, Zr, and W, have been proposed for application in sub-10 nm advanced memory processes.

In this study, TiO_2 is proposed as an alternative hardmask material to resolve major deformation problems in semiconductor patterning processes. TiO_2 exhibits a high elastic modulus, making it resistant to deformation, along with excellent corrosion resistance to oxygen-based plasma ans high etch selectivity over photoresist and carbon layers. It is also expected to exhibit superior optical properties and outgassing performance.

To enhance coverage over the spin-on-carbon (SOC) hardmask, an amorphous TiO_2 thin film was deposited using a plasma-enhanced atomic layer deposition (PEALD) process. Using tetrakis(dimethylamino)titanium (TDMAT) and O_2 plasma, an ALD window in the range of 100–250°C was identified, with a growth per cycle of 0.5–0.6 Å/cycle, and a refractive index close to 2.4. Transmission electron microscopy was employed to analyze the microstructure and composition of amorphous TiO_2. The elastic modulus of TiO_2 and its etch selectivity over SOC were estimated, confirming its suitability as a new hardmask material.

This study verifies the suitability of PEALD TiO_2 as a high-performance hardmask material, demonstrating its potential to replace Si-SOH and contribute to improved wafer yield through its superior mechanical properties.

AA-TuP-46 Machine Learning-Driven Thermal Budget Analysis for Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ Capacitors, ***Minjong Lee***, University of Texas at Dallas; *Jongmug Kang,* Kangwon National University, Republic of Korea; *Dushyant Narayan, Geon Park, Dan Le,* University of Texas at Dallas; *Seungbin Lee, Hyeonghong Min, Gwanghyeon Jang, Si Joon Kim,* Kangwon National University, Republic of Korea; *Jiyoung Kim,* University of Texas at Dallas

Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) devices have gained significant attention for their potential in non-volatile memory applications. ALD-grown HZO films exhibit robust ferroelectric properties and compatibility with back-end-of-line (BEOL) processes, making them promising candidates for next-generation electronics. However, achieving optimal ferroelectric behavior is highly dependent on annealing temperature, which influences phase formation and crystalline. Proper thermal treatment is essential for stabilizing ferroelectric performance within the orthorhombic phase, with ~400 °C identified as the optimal temperature for 10 nm HZO films.[1] Thus, precise control over the annealing process is critical for enhancing the performance and reliability of ferroelectric HZO-based devices. This study introduces a machine learning (ML)-driven thermal budget analysis to extend the range of annealing conditions explored for ferroelectric HZO devices.

Previous studies on low-temperature ferroelectricity in HZO films have shown that annealing at 300 °C for 48 hours is sufficient to crystallize the ferroelectric phase.[2] This low thermal budget process for ferroelectric crystallization is believed to be closely linked to both annealing temperature and time. However, a comprehensive exploration of all possible annealing conditions is practically unfeasible, as each experimental run incurs substantial time, cost, and additional labor and analysis expenses.[3] This challenge makes the integration of ML technologies particularly promising for improving cost-efficiency in process development by minimizing the required volume of experimental data. ML techniques provide deeper insights into a broader range of annealing conditions, even with a limited dataset. For example, while experimental data covers an annealing temperature range of 300 to 400 °C, ML analysis extends predictions to 200 to 500 °C. To further improve efficiency and robustness, this study integrates the Johnson-Mehl-Avrami-Kolmogorov (JMAK) model to correlate HZO crystallization kinetics with ML-based predictions. The combination of this model with ML optimization minimizes prediction errors and enhances the overall reliability of the ML model. The presentation will cover these promising approaches, along with electrical properties, technical methodologies, and experimental design.

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AA-TuP-47 Energy Storage Performance of Field-Induced Ferroelectric Al_2O_3-Inserted $Hf_{0.5}Zr_{0.5}O_2$ Thin Films for Electrostatic Supercapacitors, ***Jonghoon Shin***, *Dong Hoon Shin, Haengha Seo, Kyung Do Kim, Seungheon Choi, Tae Kyun Kim, Heewon Paik, Haewon Song, Seungyong Byun, In Soo Lee, Cheol Seong Hwang,* Seoul National University, South Korea

The growing global energy demand requires the development of efficient and reliable energy storage systems.[1] Electrostatic dielectric supercapacitors have attracted significant attention due to their high power density, fast charge/discharge speeds, high operating voltages, and

excellent cycling and thermal stability.[1] Identifying ferroelectric (FE) materials that maximize both energy storage density (ESD) and efficiency by achieving high saturated polarization (P_S), low remnant polarization (P_r), large breakdown field (E_{BD}), and slim hysteresis loop is crucial.[2] Achieving fast charging and discharging speeds is also essential for rapid energy storage and release.

$Hf_{1-x}Zr_xO_2$ thin films are promising candidates due to their well-established atomic layer deposition (ALD) processes, lower leakage current (bandgap: ~5.5 eV), and low crystallization temperatures (400-550 °C). Field-induced ferroelectric (FFE) materials are particularly promising for energy storage applications due to their reversible field-induced phase transition between the non-polar tetragonal phase (t-phase, space group: $P4_2/nmc$) and polar orthorhombic phase (PO-phase, space group: $Pca2_1$), enabling significant energy to be charged and discharged.[3] Consequently, FFE thin films display antiferroelectric-like double hysteresis loops in the polarization-electric field measurements, characterized by high P_s and low P_r.[3] Hence, enhancing energy storage performance requires maximizing the t-phase.

This study investigated the impact of Al_2O_3 doping on the structural and chemical characteristics, and the energy storage performance of atomic layer deposited $Hf_{0.5}Zr_{0.5}O_2$ (HZO) thin films. By adjusting the number of Al_2O_3 dopant cycles and layer insertion positions, optimized Al_2O_3-inserted HZO films achieved a record-high ESD of ~138 J cm^{-3} among $(Hf,Zr)O_2$-based thin films, with a high efficiency of ~80%. (Figure 1) The films maintained stable energy storage performance over 10^9 cycles at 6.0 MV cm^{-1} without electrical breakdown. (Figure 2) A single Al_2O_3 cycle (~0.12 nm), uniformly diffused at multiple locations within the HZO matrix, suppressed the monoclinic phase (m-phase, space group: $P2_1/c$) and stabilized the t-phase. This structure enhanced the FFE switching, decreased the hysteresis loop area, and increased the breakdown field (above ~8.0 MV cm^{-1}). In contrast, thicker Al_2O_3 layers (~0.24-0.36 nm) formed continuous, non-diffusive layers that hindered FFE t-phase stabilization. These findings highlight the critical role of precise Al_2O_3 insertion in maximizing the energy storage capabilities of HZO thin films.

AA-TuP-48 Atomic Layer Deposition of Ru-Ir Binary Alloy Thin Films for Advanced Interconnects*, Se-Hun Kwon,* ***Yeong-Seo Cho****, Myung-Jin Jung,* Pusan National University, Republic of Korea

Copper (Cu) has been predominantly used as an interconnect material in semiconductor Back-End-of-Line (BEOL) processes. However, it faces significant challenges due to a drastic increase in resistivity when the line width decreases below 10 nm. To address this issue, it is essential to develop new interconnect materials with a low Figure of Merit (FoM; $\rho_0\lambda$) and high cohesive energy compared to Cu that minimize electron scattering and reduce line resistance. Currently, single-metal candidates such as Ru, Co, and Mo has been extensively studied using atomic layer deposition (ALD) techniques as potential alternatives to Cu due to their favorable FoM characteristics and cohesive energies. However, the ALD of these single metals has shown limited improvements in resistivity compared to Cu.

Herein, therefore, we propose an alternative ALD binary alloy, Ru-Ir, as a new advanced interconnect material based on its FoM characteristics, which is capable of achieving lower resistivity than Cu at line widths below 10 nm. Since both Ru and Ir possess lower FoM values compared to Cu and share the same valence, they are expected to minimize the increase in resistivity when forming an alloy. Additionally, the Ru-Ir binary alloy has a wide solid solubility range, allowing effective control of the mean free path. To investigate this new advanced interconnect material, we systemically examined the effect of compositions and thickness on the electrical resistivity of ALD Ru-Ir binary alloy thin films. And, it was carefully compared with those of Cu interconnect material. In this presentation, the detailed optimization of ALD Ru-Ir binary alloy interconnects will be discussed with an appropriate theoretical explanations, aiming to address the resistivity increase issue of Cu at interconnect width less than 10 nm, and ultimately to develop a metallization material that outperforms Cu in future interconnect applications.

AA-TuP-49 Nanolaminated Al_2O_3/ZrO_2 film using Atomic Layer Deposition to enhance corrosion resistance on SUS304 steel*, Se-Hun Kwon,* ***Jae-Hyun Kim****,* Pusan National University, Republic of Korea

Atomic layer deposition (ALD), which utilizes self-limiting surface reactions by alternately exposing precursors and reactants to a surface, has recently been investigated as a method to form thin, defect-free films. This ALD method of thin film deposition has the advantages of precise thickness control on the nm scale, excellent step coverage on complex surface morphology, and large-area deposition, which is required in industries that use large surface area materials. In this study, Al_2O_3 and ZrO_2 laminated thin films were deposited on SUS 304 Substrates using ALD technology to improve corrosion resistance in high NaCl environments such as seawater. Using ALD technology, Al_2O_3 was deposited as an amorphous, grain-free thin film to effectively block the migration of salt, a corrosive medium, into the bulk Stainless steel under the thin film, and ZrO_2 thin films, a highly corrosion-resistant oxide material was alternately deposited between the Al_2O_3 films to form a lamination structure. To form laminated Al_2O_3/ZrO_2 thin films, one supercycle consisting of two subcycles was used for deposition. The the number of repetitions of each subcycle was adjusted to form thin films with the targeted thickness.

ALD-deposited thin films were measured using an ellipsometer, transmission electron microscope (HRTEM) and X-ray diffraction (XRD). And to evaluate the corrosion resisting performance in high-salt environments such as seawater, which is one of the many corrosive media, a potentiostatic polarization test and potentiodynamic test was conducted in 3.5 wt% NaCl electrolyte, and the corrosion properties were evaluated according to the film material, film structure, and film thickness.

AA-TuP-50 Impact of Al Gradient Doping on HfO_2 Based Metal – Insulator – Metal DRAM Capacitor*, Taelim Lee, Jungwoo Bong, Hosung Lee, Seongmin Jin, Keun Heo,* Jeonbuk National University, Republic of Korea

With the growing demand for higher data storage and faster processing, improving the capacitance of metal-insulator-metal (MIM) capacitors has become increasingly critical. This study examines the impact of aluminum (Al) gradient doping on the dielectric constant of HfO_2-based MIM capacitors. Compared to uniform doping, gradient doping more effectively promotes the transition of HfO_2 to its high-k tetragonal phase, resulting in enhanced capacitance. Various parameters, including annealing temperature, capping layers, and ALD conditions, were explored to optimize high-k performance. MIM capacitors with both gradient and uniform doping were fabricated and tested under annealing conditions of 400 °C, 500 °C, and 600 °C. The results show that gradient doping significantly reduces leakage current by an order of magnitude. While the uniformly doped capacitors exhibited a dielectric constant of ~44.7 and an EOT of 0.96 nm, gradient doping led to a dielectric constant of ~60.7 and an EOT of 0.71 nm, marking a 35.8% increase in dielectric constant and a 0.25 nm reduction in EOT. These findings demonstrate the potential of gradient doping as an effective approach to improving MIM capacitor performance for high-capacitance functional applications.

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AA-TuP-51 Aero-TiO2 Three-Dimensional Nanoarchitecture for Photocatalytic Degradation of Tetracycline*, Sebastian Lehmann, Kornelius Nielsch,* Leibniz Institute for Solid State and Materials Research, Germany*; Vladimir Ciobanu, Tatiana Galatonova, Tudor Braniste, Ion Tiginyanu,* National Centre for Materials Study and Testing, Moldova (Republic of)

One of the biggest issues of wide bandgap semiconductor use in photocatalytic wastewater treatment is the reusability of the material and avoiding the contamination of water with the material itself. In this paper, we report on a novel TiO_2 aeromaterial (aero-TiO_2) consisting of hollow microtetrapods with $Zn_2Ti_3O_8$ inclusions. Atomic layer deposition has been used to obtain particles of unique shape allowing them to interlock thereby protecting the photocatalyst from erosion and damage when incorporated in active filters. The performance of the aero-TiO_2 material was investigated regarding photocatalytic degradation of tetracycline under UV and visible light irradiation. Upon irradiation with a 3.4 mW/cm^2 UV source, the tetracycline concentration decreases by about 90% during 150 min, while upon irradiation with a Solar Simulator (87.5 mW/cm^2) the concentration of antibiotic decreases by about 75% during 180 min. The experiments conducted under liquid flow conditions over a photocatalyst fixed in a testing cell have demonstrated the proper reusability of the material.

AA-TuP-52 Enhanced Reliability and Low-Voltage Operation in $Hf_{0.5}Zr_{0.5}O_2/ZrO_2/Hf_{0.5}Zr_{0.5}O_2$ Stack Compatible with Back-End of Line Process*, Yinchi Liu, Hao Zhang, Jining Yang, Xun Lu, Shiyu Li, Yeye Guo, Yiwen Yu, Hao Zhu, Lin Chen, Hongliang Lu, Shijin Ding, Wenjun Liu,* Fudan University, China

HfO_2-based ferroelectric devices have garnered significant attention in embedded memory due to their exceptional CMOS compatibility as well as sub-10 nm scalability. Nevertheless, poor crystallization and high driving

field in Zr-doped HfO_2-based ferroelectric materials ($Hf_{0.5}Zr_{0.5}O_2$, HZO) during low temperature annealing (< 400 ˚C) make it challenging to balance ferroelectricity and reliability in practical applications. Here, the back-end of line (BEOL) compatible HZO/ZrO_2/HZO stack and the corresponding capacitors were fabricated. Compared to the conventional HZO film, the HZO/ZrO_2/HZO stack exhibits superior remanent polarization ($2P_r$) of 39.6 μC/cm^2 and 53.8 μC/cm^2 under 2 MV/cm and 4 MV/cm, respectively. By integrating ZrO_2 middle layer (ML) into HZO films, robust reliability was achieved, including a large breakdown electric field of 2.73 MV/cm in 10-year time-dependent dielectric breakdown (TDDB) lifetime, as well as excellent endurance characteristic with a $2P_r$ of 38.04 μC/cm^2 after 4.34 × 10^9 cycles at 2 MV/cm and no breakdown after 6 × 10^{10} fatigue cycles at 1.5 MV/cm. It is believed that ZrO_2 ML could introduce additional strain at a low annealing temperature below 350 ˚C and improve the proportion of the ferroelectric phase in the HZO/ZrO_2/HZO stack. Then, the thickness of the ferroelectric thin films was further scaled down to sub-6 nm. The capacitor with the sub-6 nm HZO/ZrO_2/HZO stack annealed at 400 ℃ shows a superior $2P_r$ of 26.3 μC/cm^2 under only ±1.25 V sweeping, while the conventional HZO film presents nonferroelectricity. The enhanced ferroelectricity stems from the increased ferroelectric phase proportion with ZrO_2 insertion. Moreover, the capacitor with a HZO/ZrO_2/HZO stack also achieved an excellent endurance with a $2P_r$ of 27.1 μC/cm^2 after 10^{11} cycles without breakdown and only ∼12% $2P_r$ degradation at 85 ℃. The robust reliability is ascribed to the suppressed generation of defects and domain pinning under the low operating voltage. The sub-6 nm HZO/ZrO_2/HZO stack presents great potential for BEOL compatible nonvolatile memories in advanced process nodes.

AA-TuP-53 Design of Crystalline InGaO Channels with High-Temperature Stability via Thermal ALD Process Parameter Variations, ***Hye-Jin Oh,*** Hanyang University, Korea*; Dong-Gyu Kim,* Hanyang University, Republic of Korea*; Tae Woong Cho, Hae Lin Yang,* Hanyang University, Korea*; Jihyun Kho, Yurim Kim, Bong Jin Kuh,* Samsung Electronics Co., Republic of Korea*; Jin-Seong Park,* Hanyang University, Korea

Oxide semiconductors have garnered interest as potential materials to address the issues caused by the scaling down of dynamic random-access memory devices.[1] However, high-temperature stability is a critical requirement for applying oxide semiconductors to memory devices.[2] To overcome the challenges of high-temperature instability in oxide semiconductors, it is essential to maintain a similar crystal structure regardless of the annealing temperature. Here, we proposed an optimized crystalline InGaO (IGO) film for high temperature stability by engineering atomic layer deposition process parameters, ozone concentration, and deposition temperature. Our results reveal that high-temperature stability can be secured by using elevated ozone concentrations and deposition temperatures in IGO deposition. Notably, IGO deposited at 300℃ shows little change in the main (222) intensity when annealed at 700℃ compared to 400℃, and a highly c-axis aligned (222) plane is observed. The field-effect transistor with an IGO active layer deposited at 300℃ showed minimal changes in electrical parameters after annealing at 700℃ (μ_{FE}: 58.4 to 68.7 cm^2/Vs) and demonstrated excellent PBTS stability (ΔV_{th}: 0.15 V) at 3 MV/cm, 95℃. These outcomes suggest the possibility of utilizing oxide semiconductors in memory devices that require managing high-temperature thermal budgets.

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AA-TuP-54 Advancements in ALD for DRAM: High-Performance Films for Capacitor and Electrode Applications, ***Tejinder Singh,*** Eugenus, Inc.

As DRAM technology continues to scale to meet the increasing demands of high-performance computing, artificial intelligence, and data-intensive applications, maintaining capacitance while reducing cell dimensions presents a significant challenge. The aggressive scaling of DRAM unit cells necessitates innovations in high-k dielectric materials and electrode films to ensure high charge storage capability, low leakage currents, and excellent step coverage in high-aspect-ratio structures. Atomic Layer Deposition (ALD) has emerged as the key enabler for advanced DRAM capacitor and electrode fabrication, offering precise thickness control, excellent conformality, and superior material quality.

Eugenus, a leader in ALD technology, has developed next-generation solutions for DRAM capacitor and electrode deposition, leveraging its Sierra, Lassen, and Whitney ALD platforms. These systems enable the deposition of advanced materials such as ZrO_2, HfO_2, Al_2O_3, and ferroelectric $HfZrO_x$ for high-k capacitor stacks, as well as TiN, VN, and TSN for bottom and top electrodes. The Sierra ALD system, optimized for high-step coverage metal deposition, provides excellent process uniformity and throughput for TiN/VN electrodes, ensuring low resistance and high reliability in ultra-scaled DRAM architectures. The Lassen ALD system delivers high-quality dielectric films with superior conformality and electrical performance, enabling next-generation capacitor structures with minimal leakage and high breakdown strength. Additionally, the Whitney ALD system supports MoN electrode formation and gapfill applications, further enhancing DRAM performance by reducing resistance and improving integration flexibility.

This technical presentation will be focused on film properties, characterization, and device results. Key advancements in these ALD platforms include optimized precursor delivery, multi-station process modules, and improved reactor designs for high-aspect-ratio structures exceeding 50:1. These innovations enable step coverage exceeding 95% while maintaining excellent film quality, meeting the stringent demands of advanced DRAM fabrication. This presentation will discuss the technical advancements of Eugenus ALD solutions and their impact on future DRAM scaling, providing insights into high-volume manufacturing strategies for next-generation memory devices

Author: Tejinder Singh, Ph.D, Chief Technology Officer, Eugenus, Inc

AA-TuP-55 Optimization of Low-Temperature PEALD for High-Performance TiO_2/SiO_2 Optical Coatings, ***Duy Thanh Cu,*** *Guan-Yu Ke,* National Central University, Taiwan*; Wen-Hao Cho,* Taiwan Instrument Research Institute, National Applied Research Laboratories, Taiwan*; Chien-Cheng Kuo,* National Central University, Taiwan

The study introduces a revolutionary low-temperature plasma-enhanced atomic layer deposition (PEALD) technique for fabricating high-quality, stress-minimized anti-reflective coatings (ARCs). This innovative method operates at a remarkably low temperature of 70℃, challenging traditional high-temperature deposition processes and yielding superior optical coatings with reduced residual stress.

The optimized process at 150 W plasma power produces high-quality optics with an average reflectivity of 0.35% in the visible spectrum while maintaining low stress, a significant achievement for low temperature deposited optical coatings. Focusing on titanium dioxide (TiO_2) and silicon dioxide (SiO_2) stacking using PEALD at 70℃, the research addresses high-temperature deposition challenges and mechanical stress issues for polymer substrates.

A notable stress compensation effect is observed between TiO_2 films (tensile stress ~220 MPa) and SiO_2 films (compressive stress ~-35 MPa). This combination strategy results in a remarkably low total stress of 48 MPa for multi-layer ARCs, marking significant progress in stress control for optical coatings. Interestingly, findings reveal that carbon and nitrogen incorporation into TiO_2 films occurs, with carbon doping does not have significant impact on the film absorption.

The use of common, cost-effective materials like SiO_2 and TiO_2 enhances the scalability of this approach for industrial applications. The stress-reduction effect persists even with thickness variations up to 9.6%, demonstrating real-world applicability.

These films exhibit low defect density, an amorphous structure, and surface smoothness approaching one atomic monolayer (~0.2 nm), indicating high optical quality comparable to high-temperature deposited films. This low-temperature PEALD technique not only advances optical coating technology but also expands possibilities for coating temperature-sensitive substrates and complex 3D structures, promoting applications in flexible electronics, advanced optical components, and next-generation display devices.

AA-TuP-56 Analysis of the Ambipolar Conduction of Atomic-layer-deposited Tin Monoxide Thin-Film Transistors with Indium Tin Oxide Electrodes, *Cheolseong Hwang,* ***Sahngik Mun****, Seoryong Park, Yonghee Lee, Sukin Kang, Jinheon Choi, Jaewon Ham, Juneseong Choi,* Seoul National University, Republic of Korea

The increasing demand for higher-density NAND Flash memory has driven dimensionality scaling and device structure transition from two-dimensional to three-dimensional (3D). Conventional polysilicon channel has shown deteriorated electrical characteristics as the channel thickness reached sub-10 nm in the 3D NAND Flash structure, prompting the

exploration of alternative channel materials, with metal oxide semiconductors emerging as strong candidates. For a metal oxide semiconductor to function as a channel material in NAND Flash memory, it must support the conduction of both holes and electrons because they must be injected from the channel to the charge trap layer to erase and program the cells. When adopted as a channel material in NAND flash memory, n-type oxide semiconductors such as InGaZnO have demonstrated effective electron conduction and programming capabilities. However, they lack holes, making the erase operation challenging.

Tin monoxide (SnO) is an appealing contender for this purpose due to its relatively small indirect bandgap of 0.7 eV, which allows for the contact metal's Fermi level to be close to both the conduction band minimum (CBM) and valence band maximum (VBM). In addition, the energy band structure, comprising Sn 5p orbitals at the CBM and hybridized Sn 5s and O 2p orbitals at the VBM, provides a metallic character in both band edges, facilitating the conduction of both holes and electrons.

This study explores the possibility of applying atomic-layer deposited (ALD) SnO as a channel material in 3D NAND Flash. ALD SnO exhibits intrinsic p-type conduction characteristics due to the formation of tin vacancies, which act as shallow acceptor states and generate holes. Previous research has primarily focused on utilizing ALD SnO's p-type conduction characteristics. On the contrary, the high density of defect states within the bandgap and the significant electron injection barrier limits the n-type conduction in ALD SnO thin-film transistors (TFTs).

This work modulates the source/drain (S/D) electrodes to achieve electron conduction in ALD SnO TFTs. Indium tin oxide was adopted as the S/D electrode material, enhancing electron conduction and enabling ambipolar conduction characteristics. Furthermore, a mobility extraction method under electron-hole recombination conditions is proposed. The electron-hole recombination is an unavoidable phenomenon in ambipolar TFTs, where electron and hole conduction co-occurs. Therefore, considering the application of ambipolar ALD SnO as a channel material in 3D NAND Flash, the influence of electron-hole recombination phenomena on carrier mobility was analyzed.

AA-TuP-57 Catalyst Engineering and Synthesis via Atomic Layer Deposition*, **Xinhua Liang**,* Washington University in St. Louis

Heterogeneous catalysts enable numerous chemical transformations of fossil resources (such as natural gas, methane, liquid petroleum, and coal) into useful products. Typically, heterogeneous catalysts consist of small metal particles dispersed on a high-surface-area porous oxide support. Atomic layer deposition (ALD) has primarily been used for the formation of oxide thin films with precise atomic-layer control. Due to the unique nucleation process during the first few cycles of ALD, it can also be employed to prepare highly dispersed metal nanoparticles or even single metal atoms. In this presentation, I will discuss our recent progress in the preparation of metal and bimetallic nanoparticles using ALD, as well as ALD thin film modified catalysts for various catalytic reactions, such as dry reforming of methane and selective hydrogenation.

AA-TuP-58 Enhancement of Stress Distribution through Patterned Island Design Using Atmospheric Pressure Spatial-ALD*, **Min-Seo Kim**, Won-Bum Lee, Chi-Hoon Lee, Jin-Seong Park,* Hanyang University, Korea

Wearable and flexible electronic devices are becoming increasingly important in advanced technologies, such as healthcare monitoring, wearable sensors, augmented reality (AR) displays, and next-generation communication devices. These technologies require display solutions that maintain high reliable performance under mechanical strain. However, conventional active-matrix organic light-emitting diode (AMOLED) displays often experience electrical degradation, fatigue damage under repeated mechanical deformation, posing challenges for commercialization. To overcome these limitations, this study introduces a novel island-bridge structure for oxide thin-film transistors (TFTs) fabricated using atmospheric pressure spatial atomic layer deposition **(AP S-ALD)**. Unlike conventional ALD, **AP S-ALD** enables rapid deposition with continuous precursor and reactant flows separated by inert gases, preserving ALD's self-limiting properties. It simplifies equipment needs, reduces maintenance costs, and supports flexible electronic displays with high efficiency and durability. Using this advanced deposition technique allows for accurate thickness control and excellent step coverage enabling the fabrication of high quality TFTs. Moreover, it significantly enhances mechanical stability while preserving electrical properties, making it a promising solution for next-generation electronic devices.

We evaluated the effect of pattern variation on stress distribution through ANSYS finite element analysis (FEA) simulations, using square, circular, and patterned islands further divided into 4, 8, 12, and 16 sub-patterns. The results demonstrated that circular and patterned islands reduced stress distribution compared to conventional square islands. This novel patterned island-bridge structure shows reduction of maximum stress distribution on the TFT regions. Based on these findings, oxide TFT devices were fabricated and tested using AP S-ALD to experimentally verify the results. The devices maintained stable electrical performance under 30% mechanical strain, outperforming square island designs. This enhanced strain tolerance indicates a lower risk device failure under prolonged deformation. By utilizing the patterned island-bridge structure to enhance mechanical stability, this study presents a strategic design approach for next-generation stretchable electronics.

AA-TuP-59 Demonstration of Reliable Ferroelectric Memory with Optimized 4 Nm-Thick $Hf_{1-x}Zr_{Rx}O_2$ Films and an Ultra-Thin Al_2O_3 Capping Layer*, **Han Sol Park**, Cheol Seong Hwang,* Seoul National University, Republic of Korea

Ferroelectric Zr-doped HfO_2 ($Hf_{1-x}Zr_xO_2$) thin film was recognized for its robust ferroelectric properties down to nano-scale thickness and compatibility with complementary metal oxide semiconductor (CMOS) technologies[1]. However, the widespread application of the $Hf_{1-x}Zr_xO_2$thin film as ferroelectric random access memory (FeRAM) is impeded by its high coercive field (E_C), which leads to a high operation voltage[2].Developing ferroelectric $Hf_{1-x}Zr_xO_2$ thin film operating at a voltage as low as ~1 V without compromising memory performance for highly integrated FeRAM technologies is urgently required.

The operation voltage can be decreased by decreasing the film thickness. However, when the$Hf_{1-x}Zr_xO_2$ film thickness decreases to as low as~5 nm, non-ferroelectric tetragonal phase stability increases due to the dominance of its low surface energy effect[3]. Moreover, meeting low thermal budget requirements in back-end-of-line processing becomes difficult in thinner films due to rapidly increasing crystallization temperature with decreasing thickness[4]. Such a high annealing temperature degrades the interface of the ferroelectric layer with the electrode films, undermining the reliability of thin films.

This study reports experimental optimization of the thickness scaling for $Hf_{1-x}Zr_xO_2$ thin films for stable operation at low voltage with high reliability. By adjusting ozone dose time, Zr ratio, crystallization annealing temperature, and TiN capping electrode thickness, the ferroelectric properties of the 4nm-thick film were significantly enhanced without compromising reliability. Furthermore, the high leakage current of the 4 nm-thick $Hf_{1-x}Zr_xO_2$ decreased ~10^2 times by capping an ultra-thin Al_2O_3 layer (< 5 Å). Optimized 4nm-thick $Hf_{1-x}Zr_xO_2$ thin film showed great potential in FeRAM applications with a $2V_C$ of ~0.8 V and double remanent polarization ($2P_r$) of ~25 μC/cm^2 at an applied voltage of ±1 V with a switching endurance of 10^{11}, which conforms to the giga-bit density FeRAM requirements.

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AA-TuP-60 Zirconium Carbide (ZrC_x) Thin Films as Next-generation Diffusion Barriers for Cu and Ru Interconnects Prepared by Plasma Enhanced Atomic Layer Deposition*, **Minjeong Kweon**, Chaehyun Park, Sang bok Kim, Soo-Hyun Kim,* Ulsan National Institute of Science and Technology (UNIST), Republic of Korea

Zirconium(Zr)-based materials have attracted significant interest in semiconductor applications, such as diffusion barriers, gate electrodes, and high-temperature electronic devices, due to their high thermal stability (T_m for Zr: 1850°C, ZrC: ~3420°C, ZrN: ~2980°C), low resistivities (Zr: ~42, ZrC: ~43, ZrN: ~12 μΩ·cm), and chemical stability. While the ALD (atomic layer deposition) process of zirconium nitride (ZrN) has been somewhat studied, a research on the ALD process of zirconium carbide (ZrC_x) has not been reported yet so far.In this study, we, for the first time, investigated the ALD process for ZrC_x thin film using a showerhead-type PE-ALD reactor (IOV dX1 PEALD, ISAC Research, Korea). A nitrogen-free zirconium precursor was used as the precursor, while H_2 plasma served as the reactant. The deposition was carried out at a chamber pressure of approximately 1 Torr within a temperature range of 150–450 °C. The optimal deposition

temperature was found to be 300 ℃ where a self-limiting growth was confirmed with a saturated growth rate of ~ 0.2 Å/cycle. The resistivity of ALD-ZrC_x film was as low as ~ 300 μΩ·cm with the rock-salt crystal structure.The properties of ALD- ZrC_x films deposited under optimized conditions were analyzed using various characterization techniques, including XRD, XRR, XPS, 4-point probe, RBS, TEM, and UPS. To assess the potential of ALD-ZrC_x films as practical diffusion barriers in interconnect applications, their ability to prevent the diffusion of Cu and Ru during metallization was evaluated. The results of this study highlight the potential of ZrC_x thin films for next-generation semiconductor technology and contribute to the foundation for future application-oriented research.

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AA-TuP-61 Centralized Bulk Precursor Delivery by Means of Direct Liquid Injection*, **Ehsan Mohseni**, Johannes Grübler, Joerg Koch,* SEMPA SYSTEMS GmbH, Germany

Deposition techniques such as chemical vapor deposition (CVD) and atomic layer deposition (ALD) are particularly suitable for the deposition of specific elements delivered by precursor chemicals. They achieve industrial standards for film thickness, uniformity, and purity for coatings much more reliably and reproducibly than physical deposition and wet chemical techniques. This is particularly true for depositions on 3D surfaces. Both techniques, which are used in the semiconductor, photovoltaic and optoelectronic industries, among others, require a precise and reliable supply system of precursor materials, which poses several difficulties. Only 10% of industrially available precursors are gaseous, while about 80% are in the form of powders or crystals [1]. Solid precursors are the most challenging among others because the sublimation rate is directly related to the free surface area, which changes as sublimation progresses, resulting in a non-constant mass transport rate during the deposition. In addition, most of the available precursors have safety requirements.

Non-gaseous precursors are commonly delivered by evaporation. This is conventionally realized using bubbler or vapor draw technologies, where a carrier gas passes through or by the precursor, and becomes saturated before being delivered. The vapor delivery rate depends on the temperature, pressure, and in case of the bubbler, the carrier gas flow. Increasing the latter may lead to temperature instability and fluctuations in delivery rate and precursor concentration. Because of this thermodynamic limitation, the use of bubblers is recommended when low precursor consumption is required, and typically each deposition reactor requires its own bubbler. Moreover, downstream insulation is often necessary to avoid condensation [2].

Direct liquid injection (DLI) is an alternative vapor delivery technology in which the precursor is kept at room temperature and only the required amount is vaporized and injected into the reactor [3]. Unlike bubbler technology, the supply rate in DLI is not limited by the vapor pressure. This makes it particularly interesting for precursors with low thermal stability and low vapor pressure. Fully automated with high-precision flow and pressure controllers, DLI allows high-throughput precursor supply while maintaining an adjustable concentration range both below and above atmospheric pressure level. This allows one DLI system to be used as a central supply unit for multiple reactor chambers, resulting in a compact design and reduced footprint. Here we present our latest DLI technology designed for liquid as well as solid precursors.

AA-TuP-62 Highly-Conductive ALD-WCx Thin Films Using a New Fluorine-Free W Precursor for Cu & Ru Interconnects*, **Dongbeom Seo**, Soo-Hyun Kim, Sang Bok Kim,* Ulsan National Institute of Science and Technology, UNIST, Republic of Korea

Tungsten-based materials (W, WN_x, WN_xCy, WC_x) exhibit an exceptional hardness, good chemical and thermal stability, and low resistivity. Due to these outstanding properties, tungsten-based thin films have been extensively investigated as Cu diffusion barriers, adhesion layers for interconnects, and metal gates. Tungsten-based thin films are predominantly deposited using WF_6 as a precursor for a long time. However, WF_6 generates toxic and corrosive hydrogen fluoride (HF) as a reaction byproduct. The F impurities in the deposited film result in the etching of underlying substrates and defect formation which can degrade the performance and reliability of devices. To address these challenges, the deposition of W-based thin films using fluorine-free tungsten (FFW) precursors has become crucial, and substantial research efforts are actively advancing this field. [1, 2] In this study, WCx thin films were deposited by plasma enhanced atomic layer deposition (PEALD) using a new FFW metalorganic precursor and H_2 plasma as the reactant, at the deposition temperature ranged from 200 to 300 ℃. Self-limiting growth behavior was observed for both precursor pulsing and reactant pulsing at 250 ℃ of the deposition temperature, with the saturated growth rate of approximately 0.4 Å/cycle. The ALD-WC_x film deposited at 250 ℃ was identified as a nanocrystalline structure with a face-centered cubic β-WC_{1-x} phase by XRD and XPS analyses. Remarkably, the resistivity of ALD-WC_x film at the optimized deposition condition was as low as ~190 μΩ·cm, which shows its potential for various applications including a diffusion barrier/glue layer for Cu and Ru metallization as well as a gate or capacitor electrode material for advanced 3D devices.

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AA-TuP-63 Germanium Doping for Electrical Modulation of Ferroelectric $HfZrO_4$ Using Atomic Layer Deposition*, **Jared McWilliams**, Sunil Ghimire, Charlene Chen, Ray Meck, Nguyen Vu,* Merck KGaA, Darmstadt

Since its first discovery, ferroelectricity in hafnia-based oxides has seen significant improvement using the large-scale, manufacturing-friendly atomic layer deposition (ALD) method, making them the most promising candidate for advancing non-volatile memory technology.[1] Among all compositions, the 1:1 ratio alloy $HfZrO_4$ (HZO) is the most studied compound due to the low thermal budget required to achieve satisfactory electrical performance. However, its further technical adoption has been hindered by the high operating voltage of HZO,resulting in high energy dissipation and early device failure. Significant efforts have been invested towards understanding switching mechanisms and predicting potential dopant candidates to reduce the coercive voltage of HZO. [2]

This work demonstrates, for the first time, the experimental validation of Germanium-doped HZO since the theoretical prediction by Chae *et al*.[3] Electrical behaviors such as polarization switching, leakage, and voltage-dependent capacitance are taken into account along with physical characterizations to elucidate the mechanisms behind the ferroelectric switching and the reduction in the coercive field of Ge-doped HZO. Different doping strategies to achieve desirable ferroelectric characteristics are also presented, highlighting the importance of dopant concentration and the location of dopant atoms within the device stack. The advantage of using precursors with wide ALD windows is also discussed to emphasize further the role of precursor choices in maintaining a low thermal budget for the fabrication process of doped HZO.

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AA-TuP-64 Trap Density Reduction in High-k Dielectrics: A Dual Approach with ALD Optimization and HPDA*, Taewon Hwang, *Su-Hwan Choi, Chang-Kyun Park, Jin-Seong Park,* Hanyang University, Korea

The semiconductor industry has advanced through continuous device scaling, improving speed and integration density. However, scaling introduces challenges such as short-channel effects and increased leakage currents due to tunneling in thin insulators. High-k dielectrics with permittivities exceeding Si_3N_4 (k ~7), such as Al_2O_3 (k ~9), HfO_2 (k ~25), and ZrO_2 (k ~25), have been introduced to address these issues. Al_2O_3 offers thermal stability, while HfO_2 and ZrO_2 enable tunable properties through their crystalline phases. However, defects in high-k materials—such as grain boundaries and impurities—form leakage pathways, while interface traps degrade electrical performance by increasing trap-assisted tunneling and instability. Addressing these defects is critical to enhancing device reliability.

Hydrogen annealing effectively passivates traps, reducing interface trap density and improving electrical properties. However, traditional forming gas annealing (FGA) at high temperatures can cause oxygen scavenging and structural degradation. High-pressure hydrogen annealing enhances hydrogen incorporation at lower temperatures, mitigating these issues. Deuterium annealing (D_2) also provides stronger and longer-lasting passivation due to its higher bond strength and lower diffusivity than hydrogen.

This study employs a dual approach to minimize defects: (1) optimizing atomic layer deposition (ALD) to reduce bulk defects and (2) applying high-pressure deuterium annealing (HPDA) to enhance interface stability. Increased ALD pressure and ozone flow promote Cp-ligand combustion, reducing impurities and bulk trap density. HPDA facilitates deuterium diffusion into bulk and interface regions, significantly lowering defect densities. D-SIMS confirmed successful deuterium incorporation across different high-k materials. HPDA reduced hysteresis and interface trap density for HfO_2, and ZrO_2 from 0.39 V and 3.98×10^{11}, and 0.44 V and 5.21×10^{11} $eV^{-1}cm^{-2}$ to0.38 V and 2.05×10^{11}, and 0.40 V and 5.16×10^{11} $eV^{-1}cm^{-2}$, respectively. Charge pumping confirmed that HPDA-incorporated deuterium does not contribute to mobile charge, ensuring long-term reliability.

These results demonstrate HPDA's effectiveness in defect reduction, offering a promising strategy for improving the performance and stability of high-k dielectrics in next-generation semiconductor devices.

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AA-TuP-65 ALD-Al_2O_3 Buffer Layer, a Key Component for Realizing Stretchable Thin Film Transistor Arrays*, Jaehyun Moon, *Bock Soon Na,* Electronics and Telecommunication Research Institute (ETRI), Republic of Korea*; Sangmin Lee, Taek-Soo Kim,* Department of Mechanical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea*; Seong-Deok Ahn, Seung-Youl Kang,* Electronics and Telecommunication Research Institute (ETRI), Republic of Korea

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In this work, bearing the importance of stretchability in the field of emerging electronics, we describe and demonstrate a scheme which is useful to make stretchable oxide TFT array. Integration of stiff inorganic devices on soft and compliant polymer substrates is technically demanding. In this regard, we highlighted the crucial roles of conformably ALD- Al_2O_3 buffer layer on a wavy compliant surface, which not only enables TFT processes but also mechanically withstands cyclic stretching. Substrates bearing surface waviness are advantageous to sustain externally induced strain. Rather than letting the system to evolve to bear wrinkles, it is advantageous to use a platform on which wrinkles are already formed. In this regard, we fabricated the oxide TFT array separately on a PI/glass substrate using reliable vacuum deposition and photolithographic processes. Using a laser lift off (LLO) process, the PI/TFT array was detached, and laminated on a pre-stretched compliant substrate. Upon releasing the pre-stretched substrate, a wavy PI/TFT array was formed. The mechanical properties of ALD- Al_2O_3 film of 150 nm thickness was directly measured to have a Young's modulus of ~130 GPa. TFTs on our array can withstand stain 13 % and metal buses fully conductive up to cyclic strain of 30 %.

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AA-TuP-66 Optimization of High-*k* Gate Insulators for Amorphous IGZO channel-based 3D DRAM: Materials and Process Development*, Seonyeong Park, *Jisang Yoo,* Yonsei University, Korea*; Jeongwoo Park, Pilsang Yun, Daewon Ha,* Samsung Electronics Co., Republic of Korea*; Hyungjun Kim,* Yonsei University, Korea

As device scaling accelerates, the conventional planar dynamic random access-memory (DRAM) structures are transitioning into 3D DRAM architectures. Various issues arise while converting the traditional Si-based transistors to 3D structures. For example, using single crystal Si requires over 100 layers of Si/SiGe epitaxial growth, but the complexity of 3D stacked structures makes them unsuitable for large-scale manufacturing. Polycrystalline Si, commonly used in V-NAND, faces issues like leakage current and degradation between cells due to grain boundaries. Amorphous Si offers process advantages but suffers from poor electron mobility and defects.

To address these problems, amorphous oxide semiconductors (AOS) have emerged as potential alternatives. Specifically, amorphous Indium Gallium Zinc oxide (a-IGZO) has gained attention because it can be deposited by physical vapor deposition (PVD) and atomic layer deposition (ALD), making it suitable for mass production. Additionally, a-IGZO has fewer issues with leakage current and degradation compared to polycrystalline and amorphous Si, and it meets the required electron mobility of 2~10 cm^2/Vs needed for 3D DRAM. However, research on a-IGZO has primarily focused on the channel material, while the gate insulator (GI) and source/drain (S/D) contact materials and processes remain underdeveloped.

In particular, ALD-based GI, which are preferred for their conformal deposition capability in 3D structures, face challenges when high-*k* GI directly deposited onto a-IGZO. Traditional high-*k* GIs cause leakage current due to a low conduction band offset, and direct reactions between the a-IGZO channel and ALD precursors can lead to trap states (oxidant vacancy, V_O) at the channel interface.

Therefore, our research focuses on optimizing the direct deposition of high-k GIs onto a-IGZO. We have explored various oxide materials and precursor-oxidant combinations to find the best process for reducing leakage current and improving device performance. After confirming basic ALD growth characteristics, we used techniques like X-ray photoelectron spectroscopy (XPS) and X-ray diffraction (XRD) to analyze thin film properties. We also fabricated metal-oxide-semiconductor (MOS) capacitors and a-IGZO channel field-effect transistors (FETs) to evaluate their performance.

AA-TuP-67 Polarity-Induced Threshold Voltage Shift in Ovonic Threshold Switch Device Based on Atomic Layer Deposited Germanium Selenide for Vertical Three-Dimensional Selector-Only Memory*, Jeong Woo Jeon, *Byongwoo Park, Sangmin Jeon, Sungjin Kim, Wonho Choi, Gwangsik Jeon,* Seoul National University, South Korea*; Junyoung Lim, Yonghun Sung, David Ahn,* SK Hynix, Korea*; Cheol Seong Hwang,* Seoul National University, South Korea

This study investigates the fabrication and electrical performances of vertical selector-only memory (V-SOM) devices with atomic layer deposited conformal $Ge_{0.6}Se_{0.4}$ films for scalable storage-class memory applications. The bias polarity played a crucial role in stably inducing the polarity-induced threshold voltage (V_t) shifts originated by the asymmetric contact area between the vertical tungsten bitline (BL) and tungsten wordplane (WP). When a positive voltage was applied to the BL and the WP was grounded, stable switching occurred for initial forming, resulting in repeatable V_t readings. Conversely, applying a negative voltage caused subsequent V_t values measured under positive bias to be higher than those measured only with positive bias. The read voltage value between two V_t states provided sufficient current contrast, where a lower V_t state exhibited higher current (indicating the SET state), and a higher V_t state exhibited lower current (indicating the RESET state). The memory window (ΔV_t), the

difference between the RESET and SET V_t values, showed minimal dependency on chalcogenide film thickness and cell area but increased with on-current amplitude. Cross-sectional analysis revealed polarity-sensitive elemental migration in amorphous films, driven by the electronegativity difference of Ge and Se. Compositional changes induced a gradient mobility edge, validated through subthreshold conduction analysis and subsequent modeling of field-induced non-equilibrium carrier distribution using a modified Poole-Frenkel equation. These results confirm the influence of band modulation on subthreshold conduction and ΔV_t, supporting the feasibility of the $Ge_{0.6}Se_{0.4}$ film-based V-SOM devices for vertical crosspoint architectures.

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AA-TuP-68 Designing Low-Thermal-Budget Hafnia-Based Ferroelectrics Capacitors*, **Peng Yuan**, Xufang Zhang, Jing Zhang,* North China University of Technology, China

In just over a decade, HfO_2-based ferroelectric thin films have progressed from early research stages to a potential candidate for integration into backend-of-line (BEOL) processes, with the possibility of industrialization.Acting as the dielectric in the 1T1C unit for ferroelectric random-access memory (FeRAM) or Dynamic random-access memory (DRAM), HfO_2-based ferroelectric thin film should be compatible with the thermal budget requirement (<400°C) of BEOL processes, especially in advanced nodes. However, achieving the necessary properties for these films typically requires rapid thermal annealing at temperatures above 400°C. Consequently, the pursuit of a low thermal budget (<400°C) for HfO_2-based ferroelectric materials has become a significant focus in the field. Despite this, achieving both high remanent polarization (P_r) and endurance within a low thermal budget remains a considerable challenge.

In this work,we provide a comprehensive study of atomic layer deposition (ALD) techniques for obtaining low-thermal-budget hafnia-based ferroelectric capacitors, including doping element, deposition temperature, and interface engineering. Additionally, we demonstrate ferroelectric hafnium-gallium oxide annealed at 400°C with high remanent polarization (P_r) and good endurance. Ferroelectric capacitors based on $Hf_xGa_{1+x}O_2$ thin films demonstrated high remnant polarization ($2P_r > 25\mu C/cm^2$), and good endurance for 10^9 cycles, making it fully compatible with BEOL processes.

AA-TuP-69 Low Resistivity Amorphous/Polycrystalline Titanium Nitride Multilayer Thin Films by Plasma-Enhanced Atomic Layer Deposition for Metal Diffusion Barrier*, Christophe Vallee, **Van Long Nguyen**, Natalya Tokranova,* University at Albany-SUNY

Titanium nitride (TiN) has attracted significant interest in microelectronics due to its excellent chemical resistance, thermal stability, and low resistivity. [1] It is widely used as a metal gate in CMOS technology, electrode material in DRAMs, and metal diffusion barrier. [2-4] Traditionally, TiN thin films are deposited using physical vapor deposition (PVD) or chemical vapor deposition (CVD). However, as device geometries become more complex and shrink to nanometer scale, halogen-free atomic layer deposition (ALD) processes are preferred due to their angstrom scale controllability, superior step coverage, and reduced risk of metal corrosion. To obtain low-resistivity TiN films, plasma-enhanced ALD (PE-ALD) is more effective than conventional thermal ALD due to improving TiN crystallinity and minimizing oxygen and carbon impurities. Additionally, the plasma with substrate biasing can further improve film quality thanks to the presence of energetic ions. In this study, we demonstrate a low-resistivity TiN multilayer thin film composed of alternating amorphous and polycrystalline TiN layers, deposited by using supercycles of PE-ALD (**Figure S1a**). The amorphous layers, an effective metal diffusion barrier due to its disordered structure making complex pathways for metal atoms to diffuse through, continue to interrupt diffusion pathways via grain boundaries of polycrystalline layers which have low electrical resistivity. As a result, the multilayer structure film can exhibit improved barrier properties and electrical resistivity (**Figure S1b**). The PE-ALD processes were carried out at 250°C using tetrakis(dimethylamido)titanium (TDMAT) with Ar plasma for amorphous TiN layers, and TDMAT with N_2/H_2/Ar plasma for polycrystalline TiN layers. Our initial results indicate a promising research direction; however, further investigation and optimization are required for both TiN single-layer and multilayer structures.

AA-TuP-70 Influence of Thermal Annealing on Interdiffusion and Electrical Characteristics of Ferroelectric FETs Interface of IGZO/HZO*, **HyeJoo Kang**,* Ajou University, Republic of Korea*; Seung Wook Ryu, Dohee Kim, Jongyoung Lee,* SK Hynix, Korea*; Il-Kwon Oh,* Ajou University, Republic of Korea

Due to the physical processing limitations of dynamic random access memory (DRAM) capacitors, various memory devices for capless DRAM are being explored. Among these, ferroelectric field effect transistors (Fe-FETs) using ferroelectricity properties stand out as promising candidates for capless DRAM technology. Recently, research has focused on Fe-FETs utilizing hafnium zirconium oxide (HZO) as the ferroelectric material and indium gallium zinc oxide (IGZO), known for its extremely low off-current, as the channel material.[1] However, high-temperature annealing is often required to induce the desirable ferroelectric phase in HZO. This annealing process can lead to interdiffusion of elements at the interface between the HZO and IGZO layers, potentially forming unwanted phases and defects.[2] These issues can negatively impact the electrical properties and overall performance of the devices.[3] Therefore, addressing and mitigating interdiffusion at the interface during annealing is crucial for maintaining device stability and performance. Understanding the mechanisms of interdiffusion and developing strategies to minimize its effects are essential for the reliable fabrication of Fe-FETs.[4]

In this study, we investigate the impact of annealing temperature on interdiffusion at the IGZO/HZO interface and the electrical device characteristics of Fe-FET using IGZO/HZO. To evaluate the effect of annealing temperatures ranging from 350°C to 750°C on interdiffusion at the IGZO/HZO interface, we used secondary ion mass spectrometry (SIMS) and confirmed that extreme interdiffusion occurs at temperatures above 550°C. The crystallinity of HZO, essential for its ferroelectric properties, was examined using grazing incidence X-ray diffraction (GI-XRD) on an MSFM device structured as TiN/IGZO/HZO/TiN. Additionally, polarization versus voltage (P-V) measurements were conducted on the MSFM device after annealing to evaluate its polarization characteristics. We fabricated Fe-FETs utilizing IGZO/HZO and evaluated the device characteristics, including field-effect mobility (μ_{FE}), I_{on}/I_{off}, subthreshold swing (SS) and memory window. We anticipate that this research will contribute to studies involving Fe-FETs using IGZO and HZO.

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AA-TuP-71 Plasma Enhanced Atomic Layer Deposition of HfO_2 with Applying DC Bias*, **Hee Jun Yoon**, Taeyoon Lee, Hyeongtag Jeon,* Hanyang University, Korea

As semiconductor devices become scaled down, it is important to maintain the high capacitance in dynamic random access memory (DRAM). It was studied that shrinking the thickness could increase capacitance, but it has many problems such as leakage current. Since there are limits to reducing the thickness or increasing the area, it is important to find materials with high dielectric constants to enhance the capacitance. Therefore, there are many high-k materials like Al_2O_3, and ZrO_2, but research of high k material is still being studied.[1]

Hafnium oxide (HfO_2) has been suggested as next generationhigh k material. HfO_2 has monoclinic, cubic, and tetragonal phases and the monoclinic phase has a kvalue of ~20, but the tetragonal phases has a value of ~40, therefore it is important to obtain HfO_2 with a tetragonal phase.

In the case of high-k material, it is important to deposit thin film for DRAM capacitors and the conformality, uniformity, quality must be good. Conventionally, chemical vapor deposition (CVD) has problems about requiring high temperature, poor uniformity. To meet these requirements, atomic layer deposition (ALD) has been studied for better uniformity and conformality, but plasma enhanced atomic layer deposition (PEALD) has been used for lowering process temperature and its good reactivity of radicals.[2]

However, unlike conventional PEALD, we introduced the DC bias with PEALD. When a positive DC bias is applied, the sheath region of plasma is reduced, allowing radicals to reach the substrate more easily. As a result of the high reactivity of these radicals, high-crystallinity HfO_2 can be deposited.

In this study, HfO-$_2$ was deposited using cyclopentadienyl-tris(dimethylamino) hafnium (Cp-Hf) and O_2 remote plasma. Process

window and composition of film were evaluated by spectroscopy ellipsometry (SE), auger electron spectroscopy (AES) respectively. Film density and crystallinity were evaluated by X-ray reflectometry (XRR), X-ray diffraction (XRD). X-ray photoelectron spectroscopy (XPS) was utilized for chemical binding state and analysis of step coverageain 3D structure was done with Transmission electron microscopy (TEM).

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AA-TuP-72 Development of High-Performance 2 nm In_2O_3 Thin-Film Transistors via BEOL-Compatible ALD Process Using DBADMIn Precursors*,* *In-Hwan Baek, **InHong Hwang**,* Inha University, Republic of Korea

Indium oxide has emerged as a promising channel material for thin-film transistors (TFTs), extending from display backplane applications to low-leakage DRAM transistors and monolithic 3D integrated circuits (M3D ICs) integration. The low thermal budget of atomic layer deposition (ALD) renders it compatible with M3D fabrication, thereby preventing thermal damage to underlying layers. The capability of ALD to enable conformal deposition on 3D structures has facilitated the scaling of 2T0C DRAM, demonstrating the feasibility of $4F^2$ and $2F^2$ architectures.[1] Additionally, the inherent low off-current of oxide semiconductors makes them well-suited for low-power consumption devices. In this research, we demonstrate high-performance TFTs using a 2 nm-thick indium oxide channel layer. The high mobility of the TFTs was achieved along with outstanding bias stress stability. These results highlight the scalability and applicability of indium oxide TFTs for next-generation memory devices.

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AA-TuP-73 Influence of Process Conditions on Stability and Plasma Resistance of ALD Y_2O_3 Thin Films*, **Min Joo Koo**, Hyun Mi Kim, Hye Young Kim,* Korea Electronics Technology Institute, Republic of Korea*; Chang sub Park, Yong Soo Lee,* KoMiCo, Republic of Korea*; Sung Kyu Jang, Jong Hyun Choi, Seul Gi Kim, Sun Gil Kim, Hyeong keun Kim, Ji hun Kim,* Korea Electronics Technology Institute, Republic of Korea

As semiconductor devices continue to scale down, the demand for advanced chamber coatings in etching and deposition equipment has grown. Atomic Layer Deposition (ALD) is widely used for this purpose due to its excellent film uniformity, conformality, and precise thickness control. While Al_2O_3 has been the standard chamber coating material, Y_2O_3 is gaining attention for its superior plasma resistance, high secondary electron emission, and strong etch resistance against fluorinated plasmas. However, ALD Y_2O_3 processes using H_2O as a reactant show lower reproducibility and higher variability than O_2 plasma or O_3-based processes, making it essential to address these challenges for stable film deposition.

This study developed an ALD Y_2O_3-H_2O process using a liquid precursor and analyzed the impact of process temperature on thin film properties and plasma resistance characteristics. In ALD, process temperature significantly influences film composition, surface morphology, and thickness uniformity, making its optimization crucial. To improve the reproducibility and stability of the ALD Y_2O_3-H_2O process, three approaches were employed. First, the purge time was extended to minimize the influence of residual reactive gases and byproducts remaining in the chamber after reactions. Second, an initial 40-cycle H_2O pulse-exclusive process was introduced to reduce variability in the early growth phase and stabilize the initial process conditions. Additionally, process temperature was evaluated to examine their impact on process stability and thin film formation. To ensure a comprehensive analysis, all three approaches were conducted alongside time-of-flight-mass spectrometry (TOF-MS) monitoring, which provided real-time insights into gas-phase species and reaction byproducts, aiding process evaluation. This method aimed to improve process reliability by ensuring consistency in the early growth stage. Plasma resistance evaluations were conducted using CF_4, O_2, and Ar gases gases under plasma exposure to investigate the effects of temperature variations and H2O process stabilization on the durability of Y2O3 film.

This study is expected to enhance the understanding of the Y precursor H_2O reactant process and contribute to optimizing process conditions. By improving process reliability and reproducibility, the findings can support the development of high-quality thin films for various applications.

AA-TuP-74 Increasing Quality of ALD-Grown Nitrides Through Atomic Layer Annealing*, **Bas van Asten**,* TU Delft, Netherlands

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Superconducting nitrides, such as titanium nitride, are one of the promising materials used as resonators within the fabrication of superconducting quantum computers. Typically, these resonators are used to detect and read the quantum state of qubits [1]. Through plasma enhanced atomic layer deposition these superconducting nitrides can be grown. One of the techniques proposed to increase the quality of these films is atomic layer annealing (ALA), where after every ALD cycle a thermal source is used to heat the grown layer. The effect of this anneal is similar to high temperature deposition, but has less of a toll on the thermal budget of the underlying sample. The quality of this deposition has shown to allow for low temperature epitaxial growth [2]. In this work, we characterize the superconducting TiN films by comparing the critical temperatures of films grown with ALA-ALD, using a plasma source to provide local heating. By looking at resistivity and x-ray diffraction of various films, the effects of ALA on the crystallinity of the films is investigated.

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AA-TuP-75 Plasma-Enhanced and Thermal Atomic Layer Deposition of Superconducting Nitride Thin Films*, **Zahra Ahali**,* *Sanaz Zarabi,* Beneq Oy, Finland*; Ziying Wang, Peter Liljeroth,* Aalto University, Finland*; Otto Laitinen,* Beneq Oy, Finland

Atomic layer deposition (ALD) is a promising technique for fabricating superconducting thin films with precise control on thickness and uniformity. Superconducting thin films are increasingly relevant to the semiconductor industry, where they enable advancements in ultra-sensitive sensors, cryogenic computing, and quantum technologies. Their integration with semiconductor-based devices offers new possibilities for high-speed, low-power electronics and next-generation computing architectures (1-3).

In this study, we systematically investigate the deposition of superconducting (TiN) films using both thermal ALD and plasma-enhanced ALD (PEALD) to understand how deposition conditions influence superconducting properties. By employing NH3/N2 plasma reactants, we explore the effects of key process parameters—including plasma exposure time, gas flow ratios, and plasma power—on film characteristics such as resistivity and superconducting transition temperature. The films were deposited on silicon wafer substrates and thoroughly characterized to assess their structural and electrical properties. X-ray diffraction (XRD) was used to evaluate the crystalline state of the films, while scanning electron microscopy (SEM) with energy-dispersive X-ray spectroscopy (EDX) and transmission electron microscopy (TEM) were employed to analyse film thickness and morphology (2-3).

Our results provide insights into how ALD mode impacts superconductivity in these films, highlighting the role of process parameters in optimizing superconducting performance. This study contributes to the broader understanding of ALD-based superconducting material fabrication, offering valuable data for future process optimization and material development.

Keyword: Superconducting, Thin film, ALD, Plasma, Optimization.

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AA-TuP-76 Effect of Interfacial Layer on Ferroelectricity of $Hf_{1-x}Zr_xO_2$ Thin Films in MFIS Structure, ***Hyo-Bae Kim***, *Ji-Hoon Ahn,* Hanyang University, Republic of Korea

Ferroelectrics offers new opportunities for the development of the next generation semiconductor devices such as memristors for neuromorphic computing, replacement of NAND flash, and FeFET for 2T DRAM devices. Hafnia based ferroelectrics are theoretically advantageous ferroelectrics for device scaling, due to their several advantages, such as CMOS compatibility, stable remanent polarization even below 10 nm, and unit cell-by-unit cell dipole control. Nonetheless, some challenges must be overcome to fabricate stable ferroelectrics devices, including presence of unnecessary interlayer (e.g., dead layers), and unstable ferroelectric crystallinity at thin scales. In particular, unnecessary interfacial layer contributes to the formation of depolarization fields, charge trapping/detrapping, and atomic ratio mismatches, thereby complicating the deposition of stable ultra-thin ferroelectrics. In this study, we investigated the alteration of ferroelectric properties resulting from the intentional insertion of interfacial layer between $Hf_{1-x}Zr_xO_2$ and Si substrate in MFIS structure capacitors. Measured the electrical properties and crystallinity of the thin ferroelectric capacitors (below 3 nm) and confirmed ferroelectric properties regardless of the annealing process. These results suggest that selective growth or suppress of the interfacial layer can effectively enhance the ferroelectric phase in ultra-thin films.

AA-TuP-77 Lanthanum ALD Precursors for the Application fo High-κ Gate Dielectrics, ***I-Cheng Tseng***, *Yong-Jay Lee,* Industrial Technology Research Institute, Taiwan

Rare-earth metal compounds exhibit unique electronic and magnetic properties, making them widely used in semiconductors, manufacturing, and the chemical industry. As transistors continue to shrink, rare-earth oxides are becoming increasingly important in microelectronics due to their wide band gaps, high dielectric constants, and excellent thermal stability. Atomic layer deposition (ALD) further enables transistor miniaturization.

In this study, we synthesized a lanthanum (La) ALD precursor for depositing La_2O_3 thin films, La_2O_3 has a higher dielectric constant, compare to conventional SiO_2, which can replace SiO_2 as a gate dielectric in field-effect transistor and serve as capacitor layers in next-generation dynamic random-access memory (DRAM).

AA-TuP-78 Charge Trapping Memory Structure with Low Interface Defect Density of <10^{12} cm-2 eV-1 via Remote Plasma-Based Hydrogen Post-Treatment, ***ChanHee Lee***, *Hee chul Lee,* Department of Advanced Materials Engineering, Tech university of korea

HfO_2 and ZrO_2, as high k dielectric materials, hold significant promise for replacing silicon nitride-based charge trapping layer (CTL) in conventional NAND flash memory. This potential is attributed to their high trap densities, substantial conduction band offsets relative to the tunneling oxide (TO), and thin equivalent oxide thickness (EOT). Previous studies have demonstrated that remote plasma (RP) deposition causes less damage than conventional direct plasma methods, thereby improving device performance. In our prior work, RP deposited HfO_2 and ZrO_2 exhibited a relatively low interface defect density (D_{it}) of 1.3×10^{12} cm^{-2} eV^{-1}, as measured by the Castagné–Vapaille method.

In this study, we investigate the effect of hydrogen plasma treatment (HPT) on HfO_2 and ZrO_2 to reduce D_{it} to approximately ~10^{11} cm^{-2} eV^{-1} range. Specifically, we employed remote plasma with a power of 1.9 kW at 2 Torr to activate hydrogen (5% H_2/Ar), applying a 30 second treatment for two cycles prior to high k deposition. Devices with the structure p-Si/SiO_2(~2 nm)/high-k(10 nm)/Al_2O_3(10 nm)/Au were then fabricated using either HfO_2 or ZrO_2 as the high k layer.

Capacitance–voltage (C–V) measurements were performed on these devices, and D_{it} was extracted via Berglund integration. Notably, the HPT treated devices exhibited similar C–V characteristics under both high frequency (1 MHz) and low frequency (1 kHz) conditions, indicating a very low interface defect density, especially in the shallow trap region. Furthermore, under a rapid thermal annealing (RTA) condition of 400°C for 20 minutes, ZrO_2 showed a D_{it} of 1.75×10^{11} cm^{-2} eV^{-1} and a memory window (MW, extracted using a ±4 V voltage sweep) of 0.4805 V, while HfO_2 exhibited D_{it} and MW values of 2.76×10^{11} cm^{-2} eV^{-1} and 0.4752 V, respectively.

In conclusion, our findings demonstrate that remote plasma deposition combined with hydrogen plasma treatment offers significant advantages for fabricating CTM(charge trapping memory) devices with low defect densities, achieving D_{it} values of as low as ~10^{11} cm^{-2} eV^{-1} range. Moreover, optimizing process parameters such as plasma power (which is closely correlated with radical density) and RTA conditions can make it feasible to further reduce D_{it} below 10^{11} cm^{-2} eV^{-1} and enhance the MW to above 1.5 V.

AA-TuP-79 Plasma-Pretreated ALD Growth of Platinum Catalysts on Carbon Nanotubes for Polymer Electrolyte Membrane Fuel Cell Applications, ***Junmo Koo***, Korea Maritime and Ocean University, Republic of Korea*; Joon Hyung Shim,* Korea University, Republic of Korea

Platinum (Pt) catalysts are essential for polymer electrolyte membrane fuel cells (PEMFCs), but their high-cost limits commercialization. Atomic layer deposition (ALD) provides precise control over Pt catalyst growth, optimizing efficiency and stability. This study explores the impact of oxygen plasma pretreatment on Pt ALD growth on carbon nanotube (CNT) supports. Without plasma treatment, Pt formed uniformly as small nanoparticles, whereas plasma-treated CNTs exhibited sparsely distributed larger Pt clusters due to preferential nucleation sites. Electrochemical testing revealed that catalysts grown on plasma-treated CNTs exhibited higher electrochemical surface area (ECSA) and improved fuel cell performance. The larger, well-distributed Pt particles enhanced charge transfer and oxygen reduction reaction (ORR) efficiency, leading to more stable and higher power generation compared to bare CNT-supported catalysts. Our findings demonstrate that oxygen plasma pretreatment effectively modulates Pt nucleation during ALD, improving catalyst utilization and durability. This approach provides a scalable and efficient route for optimizing Pt catalyst deposition in next-generation fuel cells.

AA-TuP-80 Impact of Zr-Precursor Ligand Design on Interfacial and Electrical Properties of ALD-Grown ZrO_2Thin Films, ***Hyeong Jun Kim***, *Haram Yang, Woongkyu Lee,* Department of Materials Science and Engineering, Soongsil University, Republic of Korea

The development of next-generation logic devices and dynamic random access memory (DRAM) capacitors requires achieving sufficient capacitance to compensate for the decreasing electrode area due to device scaling. High-k dielectric materials have emerged as a promising solution, with ZrO_2 attracting significant attention for its excellent dielectric properties: ~20 in the monoclinic phase, ~47 in the tetragonal phase, and ~37 in the cubic phase. Additionally, ZrO_2 exhibits high chemical stability and a large bandgap (~5.8 eV), contributing to stable leakage current properties. The Cp-based Zr precursor Cp-Zr(NMe_2)$_3$, primarily used for the atomic layer deposition (ALD) of ZrO_2, offers high thermal and chemical stability. However, it requires prolonged O_3 exposure time, which inevitably lead to the formation of a low-k interfacial layer by bottom electrode oxidation, degrading capacitor performance. Consequently, novel precursors have been developed for further optimized ALD process to minimize the interfacial defect formation during high-k dielectric deposition.

In this study, an ALD process using the MePrCp-Zr(NMe_2)$_3$ precursor (UP Chem Co.) and O_3 was developed, confirming ALD growth behavior across a wide process temperature range of 150-300 °C. A comparison of ALD saturation times at 300 °C between the conventional Cp-Zr(NMe_2)$_3$ and MePrCp-Zr(NMe_2)$_3$ revealed that the MePrCp-Zr(NMe_2)$_3$ exhibited higher reactivity, enabling growth of ZrO_2 thin films with shorter O_3 exposure time than Cp-Zr(NMe_2)$_3$. A planar capacitor with a (top) 60 nm Pt/ ZrO_2/ 100 nm TiN (bottom) structure was fabricated, and electrical properties revealed ~ 0.5 nm decrease in equivalent oxide thickness (EOT) when using MePrCp-Zr(NMe_2)$_3$ compared to Cp-Zr(NMe_2)$_3$. This indicates the interfacial property improvement by the suppression of the low-k TiON layer, which forms between ZrO_2 and the bottom electrode. Furthermore, etching damage of Ru substrates during ZrO_2 deposition on them using different precursors and O_3 was examined to evaluate the feasibility as next-generation electrode materials.

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AA-TuP-81 Mitigating Crystallinity Degradation and Leakage Current of Rutile TiO_2 Dielectric Thin Films via Mg Doping, ***Seungwoo Lee***, *Soomin Yoo, Chaeyeong Hwang,* Kyung Hee University, Republic of Korea*; Hansol Oh, Daeyeong Kim, Yongjoo Park,* SK Trichem, Republic of Korea*; Woojin Jeon,* Kyung Hee University, Republic of Korea

Further scaling is needed to reduce the production cost of dynamic random-access memory (DRAM), and adopting higher dielectric constant (*k*) materials as the insulators in DRAM capacitors is necessary to ensure sufficient capacitance for robust operation within limited design rules. TiO_2 is an attractive candidate due to its *k* value (>100) in the rutile phase and atomic layer deposition (ALD) compatibility but is challenged by its poor leakage current characteristics due to its low bandgap (~3 eV). For this reason, suppressing leakage current through conduction band offset control between TiO_2 and the electrode film was effective, such as Al doping. However, since ALD-grown Al_2O_3 is usually amorphous at typical ALD process temperatures, Al doping degraded the crystallinity of TiO_2, thereby reducing the capacitance density.

Therefore, in this presentation, we discuss the results of using Mg as a dopant to mitigate the crystallinity degradation of TiO_2 and induce acceptor doping effects such as Al doping. For crystallizing rutile TiO_2, we utilized MoO_2 thin films as a template and an electrode. Mg-doped TiO_2 showed a smaller decrease in *k* value with increasing doping concentration compared with Al-doped TiO_2. Grazing-incidence X-ray diffraction measurement results show that Mg doping did not significantly degrade the crystallinity of TiO_2. Additionally, the leakage current of the TiO_2 dielectric film was suppressed by Mg doping, suggesting that Mg dopant induces the acceptor doping effect like Al dopant.

Acknowledgments The authors would like to thank SK Trichem for their support and permission to publish this collaborative work.

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AA-TuP-82 Effect of Tungsten Insertion Layer on the Electrical Properties of PEALD HZO Thin Films for Semiconductor Memory Applications, *Hee Chul Lee, Ha Jeong Kim,* ***Jea Hyuk Choi***, Semicon Plasma Process LAB, Republic of Korea

Hafnium-zirconium oxide ($Hf_xZr_{1-x}O_2$, HZO)-based thin films exhibit ferroelectricity even at sub-nanometer thicknesses, making them a promising candidate for next-generation non-volatile and low-power semiconductor memory applications. However, defects such as oxygen vacancies within the HZO film can degrade its ferroelectric properties, necessitating further studies on electrode materials and processing conditions to o

In this study, Co-Plasma ALD (CPALD) was employed to deposit HZO films, and the effects of a tungsten (W) insertion layer on the electrical properties of TiN/HZO/TiN capacitors were systematically investigated. The thickness of the tungsten insertion layer was varied (0, 5, 10, and 20 nm) to examine its influence on the structural, electrical, and chemical characteristics of the HZO films. Analysis of the polarization-electric field (P-E) hysteresis curves revealed that introducing the tungsten insertion layer significantly suppressed the wake-up effect, with the highest remanent polarization (2Pr) value of 61.0 $\mu C/cm^2$ observed.

XRD analysis demonstrated that introducing the tungsten insertion layer enhanced the formation of the orthorhombic (o-) phase, which is responsible for ferroelectricity. When the tungsten insertion layer thickness increased up to 10 nm, the o-phase fraction rose from 59.1% to 81.1%, while the tetragonal (t-) phase proportion decreased. This finding strongly correlates with the observed improvement in ferroelectric performance. Furthermore, XPS analysis indicated that incorporating the tungsten insertion layer at the bottom interface reduced oxygen vacancies and improved the crystallinity of the HZO film by decreasing the proportion of sub-stoichiometric Hf 4f and Zr 3d oxide states.

A comparative analysis of electrode configurations revealed that inserting the tungsten layer at the bottom electrode resulted in superior ferroelectric properties compared to the top electrode configuration. The bottom tungsten insertion layer significantly reduced oxygen vacancies, minimizing the wake-up effect and enhancing device reliability. The highest 2Pr value was obtained when tungsten was inserted at both the top and bottom electrodes, indicating optimal ferroelectric performance.

This study demonstrates that the tungsten insertion layer plays a crucial role in improving the ferroelectric characteristics of HZO films, particularly by mitigating oxygen vacancy-related defects at the electrode interface. The electrode configuration and processing conditions proposed in this research are expected to serve as a valuable foundation for next-generation semiconductor memory technology advancements.

AA-TuP-83 The Impact of Chromium Ion Implantation on ALD Lead Chalcogenide Thin Films, *Haifeng Cong,* Old Dominion University*; Charlotte Poterie, Jean Francois Barbot,* Universite de Poitiers-CNRS, France*;* ***Helmut Baumgart***, Old Dominion University

Inherently the synthesis of semiconducting materials by Atomic Layer Deposition ALD produces only intrinsic undoped films which require the introduction of small amounts of impurities for doping to change them into extrinsic semiconductors. Apart from various in-situ diffusion doping techniques like delta doping during the ALD process, post deposition doping by ion implantation affords the best control of dose and doping profile. The present study investigates the impact of 180 keV Cr^+ ion implantation on the properties of semiconducting ALD lead chalcogenide thin films to improve their thermoelectric figure of merit. The implantation was accomplished with 180 keV Chromium ions at a given fluence of 5×10^{15} ions cm^{-2} to reach a desired 1% Cr doping level. The energy of the incident ions was tuned using stopping and range of ions in matter (SRIM) simulations to produce an implant peak around the projected range centered on the ALD film thickness. The thermoelectric PbTe thin films have been synthesized on silicon substrates covered with native oxide by ALD using lead (II)bis(2,2,6,6-tetramethyl-3,5-heptanedionato) ($Pb(C_{11}H_{19}O_2)_2$), and (trimethylsilyl) telluride ($(Me_3Si)_2Te$) as ALD precursors for lead, and tellurium and Nitrogen as the carrier and purge gas. The Si native oxide surface was functionalized before ALD PbTe thin film deposition to ensure reproducible chemisorption of the ALD precursor compounds. The growth temperature during ALD was varied over a range from 130°C to 170°C. The Lead precursor was volatilized at a temperature of 170 °C and the Tellurium precursor was heated at 45 °C. The chamber base pressure was kept at 500 mTorr.Several physical characterization techniques among them SEM and EDS have been employed to determine the ALD PbTe thin film characteristics before and after Chromium ion implantation. X-ray diffraction analysis reveals that the films exhibit a polycrystalline structure with simple cubic crystallites. Atomic force microscopy analysis was employed to determine the surface properties of the films, including surface topology, root mean square (RMS) roughness, grain height, and average size. For the electrical characterization we report the effects of the ion implantation on the resistivity ρ(T) as a function of temperature, the electrical conductivity, the Hall mobility, and the Seebeck coefficient.

AA-TuP-84 Atomic Layer Deposition of Zirconia and Titania Inhibit Sintering in Pt Catalysts Under Oxidative Reaction Conditions, ***Bang Nhan***, Department of Chemistry, Stanford University*; Shyama Mandal,* Department of Chemical Engineering and SUNCAT Center for Interface Science and Catalysis, Stanford University*; Jacob Smith,* Oak Ridge National Laboratory*; Gennaro Liccardo,* Department of Chemical Engineering and SUNCAT Center for Interface Science and Catalysis, Stanford University*; Sydney Richardson,* Mechanical Engineering, Stanford University*; Frank Abild-Pedersen,* SLAC National Accelerator Laboratory*; Miaofang Chi,* Oak Ridge National Laboratory*; Matteo Cargnello, Stacey Bent,* Department of Chemical Engineering and SUNCAT Center for Interface Science and Catalysis, Stanford University

Platinum-group elements are widely used in heterogeneous catalysis due to their exceptional activity, making them essential for applications such as emission control and electrocatalytic hydrogen evolution reaction (HER). However, their scarcity necessitates strategies to optimize metal utilization and enhance catalyst stability. Under extreme thermal and oxidative conditions, small Pt nanoparticles (NPs) sinter over time, leading to catalyst deactivation and subsequently, metal efficiency reduction.

Several strategies have been implemented to minimize sintering, such as encapsulating Pt NPs within a metal oxide framework. However, full control over the encapsulation process is still needed. Atomic layer deposition can meet the needs for growing conformal thin films with Angstrom-level precision on high-aspect-ratio substrates. In this study, we explored ALD-grown zirconia and titania as encapsulation shells for Pt catalysts. Colloidally synthesized Pt NPs were first supported on amorphous alumina (Pt/Al_2O_3), followed by ALD growth of zirconia [tetrakis(dimethylamino) zirconium and water] and titania [tetrakis(dimethylamino) titanium and water] overlayers, achieving a GPC of 1.4 Å/cycle for both processes.

The hydrothermal stability of the ALD-modified catalysts was evaluated using propene (C_3H_6) oxidation as a model reaction for residual hydrocarbon combustion. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM)revealed that after hydrothermal aging at 850°C for 4 hours, the particle size of the ALD-coated

catalysts remained unchanged, while the control Pt/Al_2O_3 catalyst experienced significant sintering. Arrhenius plots collected at steady-state C_3H_6 conversion showed that the ALD-modified catalysts exhibited improved stability and enhanced activity, whereas the control catalyst lost up to fivefold of its initial activity. Diffuse reflectance infrared Fourier-transform spectroscopy (DRIFTS) indicated that this improvement stems from the formation of under-coordinated Pt sites as small nanoclusters within the ALD overlayers during thermal aging. The enhanced stability is attributed to the physical barrier imposed by the ALD coatings, which suppresses Ostwald ripening of oxidized Pt species under reaction conditions. The zirconia-based catalysts show higher activity than the titania-based catalysts, a difference attributed to the microstructure of the ZrO_2 film. Overall, these findings highlight the effectiveness of ALD-grown zirconia and titania overlayers in stabilizing Pt catalysts, offering a promising strategy for enhancing catalyst durability and performance in high-temperature applications

AA-TuP-85 Thin Conductive Cu Films by Post-Reduction of Atomic Layer Deposited CuO, ***Maria Gabriela Sales***, *Neeraj Nepal, Peter Litwin, David Boris, Scott Walton, Virginia Wheeler,* U.S. Naval Research Laboratory

Interconnect applications in microelectronics has helped spur the need to develop robust and scalable atomic layer deposition (ALD) processes for copper (Cu). For this application space, the unique advantage of ALD is being able to conformally coat high aspect ratio via structures due to its self-saturating nature and precise thickness control. Reported ALD recipes for pure Cu typically rely on reactions between a metal-organic Cu precursor and a reducing reactant, including different chemical compounds for thermal ALD or a reducing plasma for plasma-enhanced ALD (PEALD). However, these conventional Cu ALD processes have very low growth rates of 0.1-0.5 Å/cycle, at best. As is typical of other metal ALD recipes, traditional ALD of metallic Cu requires the deposition of at least 20-40 nm in order to achieve full grain coalescence and a conductive film.

In this work, we report on an alternative way of obtaining conductive Cu films through the use of an in-situ plasma reduction. Initially, copper (II) oxide, or CuO, is deposited by PEALD at a substrate temperature of 150 ºC, using copper(I)-N,N'-di-sec-butylacetamidinate ($[Cu(^sBu\text{-}amd)]_2$) and Ar/O_2 plasma as precursors. The growth rate for this CuO recipe is 0.3 Å/cycle, which is higher than what is obtained for pure Cu using the same precursor (0.1 Å/cycle). Grown CuO films have a low concentration of incorporated ligands and a smooth surface morphology. Following CuO ALD, the CuO film is exposed to reducing plasma pulses containing a mixture of Ar and H_2 gas. This reduction with Ar/H_2 plasma exposure is performed in-situ, without removing the CuO sample from the ALD reactor. To characterize the films, spectroscopic ellipsometry (SE), X-ray photoelectron spectroscopy (XPS), atomic force microscopy (AFM), and contactless sheet resistance measurements were performed.

In this talk, we will discuss various parameters in the Ar/H_2 reducing plasma, such as total exposure time, pulse lengths, and number of reducing plasma cycles, and investigate how they affect key properties of the resultant Cu film, such as chemistry, morphology, and resistivity. Additionally, we report on utilizing supercycles of CuO ALD and reducing plasma pulses to grow thicker (30 nm) Cu films with low resistivity. To date, our most optimal CuO-then-post-reduction procedure yielded a 30 nm Cu film with a root mean square (RMS) roughness of 3.3-3.5 nm and a resistivity of 3.8 μΩ cm, which is only a factor of 2 greater than for bulk Cu.

AA-TuP-86 Enhanced Dielectric Properties of HfO2 Thin Films Produced Via Novel Catalytic Atomic Layer Deposition Process, ***Sara Harris***, *Dane Lindblad, Aaron Wang, Arreliane Dameron, Matthew Weimer,* Forge Nano

Optimized high-κ dielectric materials are widely utilized as gate oxides and dielectric barriers in compound semiconductor devices such as GaN HEMT and MEMS [1]. Monolithic high-κ dielectric materials have inherent performance tradeoffs demonstrated by hafnium oxide (HfO_2) which has a high dielectric constant but a low breakdown voltage and high leakage current limiting overall efficacy as a dielectric barrier[2]. Composite materials such as $HfAlO_x$ can improve dielectric performance by combining the high dielectric constant of HfO_2 with the wider band gap and higher breakdown voltage of aluminum oxide (Al_2O_3) unlocking capabilities for next generation dielectric materials [2]. Atomic layer deposition (ALD) exploits precise control over self-limiting surface chemistry allowing for discreet nanolayers that can be tailored to optimize bulk film dielectric performance with a level of control that is not possible via other deposition techniques (CVD and PVD). This work demonstrates HfO_2 thin films deposited via ALD with enhanced dielectric properties achieved through the addition of a novel catalytic conversion step known as a CRISP Process. HfO_2 deposited via the CRISP process has 29% higher GPC, 7% higher density, more ideal stoichiometry, 44% less carbon impurity and larger crystal grains when compared to films growth with O_3 alone. In pursuit of high performing dielectric materials several compositions of ALD deposited nanolaminates were studied through the incorporation of small amounts of Al_2O_3 into bulk HfO_2. Discreet nanolayer formation is demonstrated via cross sectional scanning electron microscopy (SEM) shown in Figure 1. With varying amounts of Al_2O_3, dielectric constant, κ, can be increased from 16.2 to 19.2, the dielectric strength (breakdown voltage) can be increased from 6.9 to 7.8 MV/cm, and the leakage current density can be reduced from $3.3x10^{-9}$ to $8.1x10^{-12}$ J at 60Vm. Figure 2 demonstrates leakage current density and dielectric constant improvements for various compositions of CRISP and ozone based HfO_2 nanolaminate thin films. Work is ongoing to tune layer composition for the best overall performance. In the future, full characterization in GaN HEMT devices is planned for both the $HfO_2 – O_3$ and HfO_2 – CRISP processes.

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AA-TuP-87 MoO2Cl2: how the first large volume solid precursor has been enabled for HVM, ***Jeffrey Yoder***, Air Liquide

The semiconductor industry is adopting Molybdenum (Mo) to replace Tungsten for some leading edge device applications to improve performance across NAND, logic, and DRAM. MoO2Cl2 is being chosen for the largest volume application in 3D NAND manufacturing due to its high vapor pressure and superior ability for word line gap-fill. In a first-of-its-kind development for a solid precursor, bulk vapor delivery systems enable the distribution of the molecule from the sub-fab to the process tools versus the use of small packaging installed inside the tool. The use of bulk systems serves to lower the customer total cost of ownership (TCO) while freeing up the valuable fab tool deck space. This talk will review the key aspects of the MoO2Cl2 application, manufacturing, supply chain, and enabling high volume manufacturing with sub-fab bulk vapor delivery systems.

AA-TuP-88 Mitigation of Surface Dielectric Loss in Superconducting Quantum Devices via Combined Atomic Layer Etching and Deposition, ***Neha Mahuli***, *Joaquin Minguzzi, Jiansong Gao, Omar Reyna, Sandra Diez, Victor Ly, Guillaume Marcaud, Matthew Hunt, Jefferson Rose, Loren Swenson, Oskar Painter, Ignace Jarrige,* Amazon

We present a surface treatment that integrates atomic layer etching (ALE) and atomic layer deposition (ALD) to mitigate the dielectric loss in superconducting quantum devices. We report the application of this dry process to aluminum (Al)-based coplanar waveguide resonators and transmon qubits. We show that ALE of Al_2O_3 at 300ºC, performed using alternating exposures of trimethylaluminum (TMA) and HF-pyridine, not only conformally removes the native metal oxide but also effectively cleans the surface by eliminating organic residues from all exposed regions, including sidewalls and silicon (Si) surfaces. Subsequent ALD of Al_2O_3 at the same temperature enables controlled regrowth of a uniform, high-purity dielectric on the metal surfaces. Our characterization of the surface chemical properties points to a significant reduction in fabrication-induced contamination and the formation of a thinner, Al-rich oxide layer that resembles pristine native Al oxide. We show that the application of this treatment to our devices is correlated with a reduction in dielectric loss at single-photon power levels by a factor of two, achieving transmon coherence times exceeding 0.4 ms — the highest reported for this geometry to date. Ongoing work aims to extend this approach to remove the native Si oxide, explore alternative low-loss dielectric encapsulation layers, and further isolate the individual contributions of ALE and ALD to these performance gains.

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