Atomic Layer Etching
Room Samda Hall - Session ALE1-WeM

Plasma and/Energy-Enhanced ALE + Sustainability

Moderators: Jane P. Chang, University of California, Los Angeles, **Sung-Il Cho**, Samsung Electronics

8:00am **ALE1-WeM-1 Centering Sustainability in Future Plasma-Enhanced ALE Processes***, Nathan Marchack, Robert Bruce,* ***Eric Joseph,*** IBM Research Division, T.J. Watson Research Center **INVITED**

Recent progress in the field of artificial intelligence has also highlighted the critical role of semiconductor manufacturing in delivering the necessary compute requirements. Simultaneously, the prospect of future proliferation of such technologies presents serious ramifications for the environment. Examinations of the increases in resource consumption as both software [1] and hardware [2] advance have raised awareness of the need to consider the sustainability of future development. In this talk we will examine this idea as it pertains to plasma-enhanced atomic layer etching (PE-ALE), building off our recent work on reducing gas usage in deep Si etching. [3] We review new results studying mechanisms of halogen substitution on Si surfaces and the need for synergy between all facets of the development process, from substrate materials to gas precursor development. Adopting this focus as soon as possible will strengthen the fundamental role of atomic layer processes in enabling future technologies.

[1] E. Strubel et al., Energy and Policy Considerations for Deep Learning in NLP, Proc. of the 57th Annual Meeting of the Association for Computational Linguistics, 2019, pp. 3645–3650, Florence, Italy.

[2] M.G. Bardon et al., DTCO including sustainability: Power-performance-area-cost-environmental score (PPACE) analysis for logic technologies, IEEE International Electron Devices Meeting (IEDM), 2020, pp. 41.4.1-41.4.4, San Francisco, CA, USA.

[3] O. Isowamwen et al., Characterization of TSV Etch from a Sustainability Standpoint, Proc. SPIE 12499, Advanced Etch Technology and Process Integration for Nanopatterning XII, 2023, 124990H, San Jose, CA, USA.

8:30am **ALE1-WeM-3 Cryogenic Atomic Layer Etching of SiO_2 by Physisorption of HF/C_2H_5OH and Ar Plasmas***, Shih-Nan Hsiao, Makoto Sekine,* Nagoya University, Japan*; Yoshihide Kihara,* Tokyo Electron Miyagi Limited, Japan*; Masaru Hori,* Nagoya University, Japan

The continues reduction of the chip size and development of innovative 3D integrated device architectures have required the adoption of advanced processing methods. Plasma-assisted atomic layer etching (PE-ALE) has emerged as a promising technique for sub-nanoscale material removal in semiconductor processes due to its unique self-limiting surface reactions. Cryogenic plasma etching enabling the unique feature of physisorption of neutrals/condensed layer has been reported for ALE of dielectric materials [1]. Our recent reports indicates that the cryogenic plasma etching can significantly enhance the etching throughput of SiO_2 through the co-adsorption of H_2O/HF species using the CF_4/H_2 gases [2]. Building on this, we developed the cryogenic ALE (Cryo-ALE) process involving an HF dose for surface modification and Ar ion bombardment for SiN etching. This work extends the Cryo-ALE process to SiO_2, utilizing an HF/C_2H_5OH dose for etchant physisorption followed by an Ar ion bombardment. *In situ* monitoring techniques, including spectroscopic ellipsometry and attenuated total reflectance Fourier transformation infrared spectroscopy (ATR-FTIR), were used to analyze the surface structure and etching characteristics. The substrate temperature (T_s) was controlled from 20 to –60 °C using a coolant circulating system connect to the bottom electrode. The etched depth per cycle (EPC) of the SiO_2 after the process increased from approximately 0.28 nm/cycle to 0.79 nm/cycle as the T_s was decreased from 20 to –60 °C. (see supplemental document for details). ATR-FTIR analysis revealed that this increase in EPC correlates with an enhanced amount of surface-adsorbed HF/C_2H_5OH during the surface modification step. Conversely, the EPC vs T_s for the SiN exhibited an opposite trend, indicating that the etching selectivity between SiO_2/SiN can be effectively tuned by adjusting T_s.

[1] D. N. Shank et al., J. Vac. Sci. Technol. A 41, 052601 (2023).

[2] S. N. Hsiao et al., Small Methods, 2400090 (2024).

[3] S. N. Hsiao et al., Chem. Mater. 36, 11042 (2024).

8:45am **ALE1-WeM-4 Cryogenic ALE of SiO_2 using CF_4 Plasma***, Madjid Adjabi, Jack Nos, Sylvain Iseni,* GREMI - CNRS/Orleans University, France*; Gilles Cunge, Martin Kogelschatz,* LTM - CNRS/Grenoble Alpes University/Grenoble-INP, France*; Philippe Lefaucheux, Loïc Becerra,* GREMI - CNRS/Orleans University, France*; Emilie Despiau-Pujo,* LTM - CNRS/Grenoble Alpes University/Grenoble-INP, France*;* ***Thomas Tillocher****, Rémi Dussart,* GREMI - CNRS/Orleans University, France

Cryogenic Atomic Layer Etching of SiO_2 ("Cryo-ALE") has been developed several years ago to address some limitations when it is performed at room temperature.The ALE process achieved under these last temperature conditions involves a C_4F_8 plasma in the modification step. This results in fluorocarbon deposition on the reactor walls, and eventually to process drifts, which affects reproducibility. Consequently, chamber cleaning is necessary. This can be addressed by flowing C_4F_8 in gas phase and cooling the SiO_2 substrate at cryogenic temperature. C_4F_8 molecules are physisorbed only on the cooled surface and therefore, wall pollution is greatly reduced. The thin physisorbed C_4F_8 layer is then used as a reservoir to etch around one SiO_2 monolayer in the subsequent Ar plasma of one ALE cycle.

Alternatively, a relevant approach consists in selecting a gas with a higher F/C ratio, which polymerizes much less than low F/C ratio gases such as C_4F_8. For instance, a CF_4 plasma is in etching regime at room temperature and does not promote polymer deposition on the chamber walls at room temperature too. Nevertheless, it is shown by absorption spectroscopy that the sticking coefficient of CF radicals increases dramatically when the surface is cooled at cryogenic temperature. This means that a CF_4 plasma can be used to deposit a fluorocarbon layer only on cooled surfaces, in particular SiO_2. But the chamber walls, at room temperature, are polymer-free.

Consequently, a CF_4 plasma can be used as a modification step in a SiO_2 Cryo-ALE process. It is demonstrated that repeating cycles of a CF_4 plasma step followed by an Ar plasma with low energy ion bombardment, with each cycle separated by a purge step, enables sequential etching of SiO_2 cooled at cryogenic temperature. The EPC increases as the substrate temperature decreases and reaches 0.46 nm/cycle at -130°C. This process, provided deposition during CF_4 plasma is well balanced with etching in the Ar removal step, exhibits a high synergy that can approach 100%.

Acknowledgments: The authors thank Tokyo Electron Limited for financial support and helpful discussions and acknowledge ANR, which supports the project PSICRYO for "Understanding Plasma-Surface Interactions in CRYOgenic etching for advanced patterning applications" (No. ANR-20-CE24-0014). This work was also supported by CERTeM platform, which provides most of the equipment.

9:00am **ALE1-WeM-5 Atomic Layer Etching of Indium Oxide Thin Films via Ligand Addition and O_2 Plasma Reactions***, Minchan Kim, Jihyun Gwoen, Hae Lin Yang, Jin-Seong Park,* Hanyang University, Korea

The Oxide semiconductors (OSs), which utilize materials like IGZO as channel layers, have been gaining increased attention as the demand for high mobility and low off - current in semiconductor devices continues to grow.Especially, InOx is emerging as a key material for next-generation devices due to its outstanding electron mobility. Achieving these characteristics requires high-quality thin films, which can be precisely and uniformly fabricated using atomic layer deposition (ALD), a technique essential for high-mobility InOx and next-generation device applications. While ALD enables precise deposition, achieving the desired crystallinity in InOx at low thickness remains challenging due to issues like nucleation and non-uniform film growth. To address this, an etch-back process using Atomic Layer Etching (ALE) is often employed, depositing the film to the required properties before selective removal. However, in the case of InOx, the low volatility of modified byproducts like $InCl_3$ or InF_3 makes their removal chemically difficult, posing significant limitations to the applicability of ALE technique

In this study, we explored the operation of Atomic Layer Etching (ALE) for InOx by incorporating an additional hydrogen treatment modification step into the conventional ligand-based ALE process using Hacac (acetylacetone). The process was evaluated through Spectroscopic Ellipsometry (SE), X-ray Photoelectron Spectroscopy (XPS), and X-ray Diffraction (XRD) to determine whether the ALE cycles proceeded in a layer-by-layer manner driven by self-limiting reactions. The findings showed that the thickness of the indium oxide thin film could be controlled with precision, while an improvement of approximately 37% in RMS roughness was observed, indicating better film quality after the ALE process.

Furthermore, XPS and XRD analysis confirmed that the bulk chemical composition remained unchanged following the hydrogen modification step, suggesting that the mechanism effectively induced reactions at the surface level. These results provide useful insights into controlling oxide semiconductor deposition and improving thin-film quality for potential device applications.

9:15am **ALE1-WeM-6 Development of a Novel Magnetically-Confined Plasma Source for Advanced Semiconductor Manufacturing**, *Tae S Cho,* Wonik IPS*; Jihyun Kim, **Giwon Shin**, Hakmin Kim, Jeonghun Kim, Sooyoung Hwang, Jaehoon Choi,* Wonik IPS, Republic of Korea

The relentless pursuit of miniaturization in the semiconductor industry, characterized by sub-10 nm feature sizes, 3D stacked architectures, and complex gate-all-around (GAA) structures, demands increasingly sophisticated plasma processing techniques. These advanced applications require plasma sources capable of operating over a broad pressure range while providing a high radical density with minimal ion-induced damage to delicate device structures.

To address these critical requirements, we have developed a novel ignitor-free remote plasma source utilizing a magnetic core configuration. Preliminary test with argon and argon-nitrogen gas mixtures demonstrates a stable operating pressure range of 0.1 to 17 Torr and 0.1 to 4.5 Torr, respectively.

Furthermore, this source exhibits a unique capability for plasma mode transition. By adjusting the magnetic core's winding ratio, the plasma can be dynamically transitioned between voltage mode and current mode operations. This flexibility allows for optimized process control, enabling the generation of high radical density for rapid etch rates in current mode, while minimizing ion bombardment for delicate deposition processes in voltage mode. Optical emission spectroscopy (OES) measurements confirm a significant enhancement in radical density in current mode compared to voltage mode.

Based on these promising results, ongoing efforts are focused on optimizing the plasma reactor, magnetic core geometry, and radio frequency (RF) generator to further enhance the performance and versatility of this innovative plasma source for advanced semiconductor manufacturing applications.

Author Index

Bold page numbers indicate presenter

— A —
Adjabi, Madjid: ALE1-WeM-4, 1
— B —
Becerra, Loïc: ALE1-WeM-4, 1
Bruce, Robert: ALE1-WeM-1, 1
— C —
Cho, Tae S: ALE1-WeM-6, 2
Choi, Jaehoon: ALE1-WeM-6, 2
Cunge, Gilles: ALE1-WeM-4, 1
— D —
Despiau-Pujo, Emilie: ALE1-WeM-4, 1
Dussart, Rémi: ALE1-WeM-4, 1
— G —
Gwoen, Jihyun: ALE1-WeM-5, 1
— H —
Hori, Masaru: ALE1-WeM-3, 1
Hsiao, Shih-Nan: ALE1-WeM-3, **1**
Hwang, Sooyoung: ALE1-WeM-6, 2
— I —
Iseni, Sylvain: ALE1-WeM-4, 1
— J —
Joseph, Eric: ALE1-WeM-1, **1**
— K —
Kihara, Yoshihide: ALE1-WeM-3, 1
Kim, Hakmin: ALE1-WeM-6, 2
Kim, Jeonghun: ALE1-WeM-6, 2
Kim, Jihyun: ALE1-WeM-6, 2
Kim, Minchan: ALE1-WeM-5, **1**
Kogelschatz, Martin: ALE1-WeM-4, 1
— L —
Lefaucheux, Philippe: ALE1-WeM-4, 1
— M —
Marchack, Nathan: ALE1-WeM-1, 1
— N —
Nos, Jack: ALE1-WeM-4, 1
— P —
Park, Jin-Seong: ALE1-WeM-5, 1
— S —
Sekine, Makoto: ALE1-WeM-3, 1
Shin, Giwon: ALE1-WeM-6, **2**
— T —
Tillocher, Thomas: ALE1-WeM-4, **1**
— Y —
Yang, Hae Lin: ALE1-WeM-5, 1