ALD Applications

Room Hall 3D - Session AA1-TuM

Applications in ULSI BEOL: Interconnects, Diffusion Barriers, & DRAM

Moderators: Mike McSwiney, Applied Materials, **David Towner**, Intel Corp.

8:00am **AA1-TuM-1 Leakage Control of DRAM High-k Capacitor Stack by Ald Sc_2O_3, Y_2O_3 Inter-Layer**, ***Randall Higuchi***, *A. Babadi, C. Chen, B. Zope,* Merck KGaA, Darmstadt, Germany

The scaling of DRAM devices and subsequent increase in memory density requires shrinking memory cell size, which necessitates engineering of the capacitor and transistor of the memory cell. Scaling of capacitor presents challenges in size shrink capacitor size and area shrinking, and reduction in number of stored charges. These factors contribute to increase in capacitor leakage, wherein it is critical to maintain leakage current <10^{-7} A/cm^2 at the operating voltage [1].

ALD oxide films of Hf & Zr, when crystallized to non-monoclinic phase have high dielectric constant, and, therefore, utilized in the DRAM capacitor stack to achieve high capacitance. However, grain boundaries of these crystalline films form dominant carrier conduction paths leading to increased leakage current. Amorphous, thin ALD Al_2O_3 layer in the middle of the high-k stack is known to engineer grain boundary structure in the film creating tortuous carrier conduction path leading to lower leakage current [1]. In this work, we investigated alternate oxide materials for inter-layer that improve leakage performance of the capacitor stack compared to Al_2O_3 inter-layer. Our work demonstrated that ALD Sc_2O_3 or Y_2O_3 can be utilized as inter-layer in the DRAM high-k stack. ALD Sc_2O_3 resulted in 33% improvement and ALD Y_2O_3 resulted in 50% leakage current improvement compared ALD Al_2O_3 (deposited using trimethyl aluminum) inter-layer. Additionally, both Sc_2O_3 and Y_2O_3 inter-layer resulted in lower EOT increase compared to Al_2O_3.

References:

[1] Jeon, W. (2020), Journal of Materials Research, 35(7), 775-794

8:15am **AA1-TuM-2 ALD Deposited IGO with High Thermal Stability (~ 800 °C) by Controlling Crystallinity for Multi-bit Operation 2T0C DRAM**, ***Jae-Hyeok Kwag***, *S. Choi, J. Sim, T. Cho, C. Park, Y. Song, J. Park,* Hanyang University, Republic of Korea

The 2T0C DRAM has advantages compared to conventional Si channel 1T1C in terms of high cell density (~ 6F^2), long retention time (> 400 s), and multi-bit operation using the current sensing mode [1-2]. Oxide semiconductors (OS) have advantages such as extremely low off current (< 10^{-18} μA/μm) [3]. Recently, capacitor-less 2T0C DRAM using a low off-current IGZO (In-Ga-Zn-O) channel was proposed. Since the FEOL fabrication includes a high-temperature process, high thermal stability is required to apply OS channel FET to DRAM. However, the electrical properties of the OS channel FET degraded above the 400 °C post-annealing process [4]. In general, Ga doping improves the thermal stability of OS. Among the various deposition methods for OS, atomic layer deposition (ALD) is a promising candidate because of its characteristics that allow easy doping concentration adjustment and easy sub-nanometer scale thickness control.

In this study, thermal stability (~ 800 °C) of Ga-doped InO channel FET was verified by controlling the thickness using the ALD method, and the 3-line based multi-bit operation of the 2T0C DRAM was confirmed. First, the InO channel FET was evaluated. The 250 °C deposited 3-nm thick InO using DBADMIn precursor was adopted to the channel layer. The c-axis aligned C(222) crystalline InO FET exhibits superior electrical properties by lowering the grain boundary effect [5] but degraded after 800 °C post-annealing for 3 hours, as shown in **Fig 1.**.To achieve high thermal stability, InO was doped with Ga using the ALD super-cycle method. The thickness of Ga-doped InO (IGO) was also evaluated because it is responsible for crystallinity. As shown in **Fig 2.**, Above the 10 nm thickness of the IGO channel, FET exhibits superior thermal stability even after the post-annealing process at 800 °C for 3 hours. The 800 °C post-annealed 10 nm thick IGO FET was adopted because the on-current and field-effect mobility were similar to 400 °C post-annealed InO channel FET (InO: 55.5 cm^2/Vs, IGO: 58.9 cm^2/Vs). As shown in **Fig 3.**, the current sensing multi-bit operation is exhibited regardless of channel material, and the RBL current has similar values according to the WBL voltage because the mobility is similar with InO and IGO channel FET.

References

[1] Duan, Xinlv, et al. *IEEE Transactions on Electron Devices* 69.4 (2022): 2196-2202.

[2]Belmonte, A., et al. *2020 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2020.

[3]Kamiya, Toshio, Kenji Nomura, and Hideo Hosono. *Science and Technology of Advanced Materials* (2010).

[4] Jeong, Hyun-Jun, et al. *ACS Applied Electronic Materials* 4.3 (2022): 1343-1350.

[5] Choi, Su-Hwan, et al. *Nano Letters* (2024).

8:30am **AA1-TuM-3 Improving Electrical Properties of ZrO_2 Dielectric Films Without Sacrificing Tetragonal Crystallinity via Gd Doping**, ***Seungwoo Lee***, *Y. Choi, J. Jeong, J. Nam,* Kyung Hee University, Republic of Korea*; H. Oh, H. Kim, Y. Park,* SK trichem, Republic of Korea*; W. Jeon,* Kyung Hee University, Republic of Korea

ZrO_2 has been used as an insulator film for dynamic random-access memory capacitors for a long time due to its compatibility with TiN electrodes and the high maturity of the atomic layer deposition (ALD) process. Tetragonal ZrO_2 thin films with a high dielectric constant (~40) on TiN electrodes could be obtained relatively easily by ALD. However, there are limitations to using only ZrO_2 due to the leakage current problem. The inevitably present grain boundaries acted as the dominant carrier conduction path. Al-doped ZrO_2 effectively suppressed leakage current by reducing the grain size and inducing a winding conduction path, but it also caused the crystallinity of ZrO_2 to deteriorate. Therefore, further scaling requires new dopants that can replace the role of Al without sacrificing the tetragonal crystallinity of ZrO_2.

In this regard, this presentation discusses the results of employing Gd as a dopant to replace Al. The Gd_2O_3 ALD process for doping in ZrO_2 was designed utilizing a novel Gd precursor. We investigated the effectiveness of Gd as a dopant for ZrO_2 by fabricating metal–insulator–metal capacitors with Gd-doped ZrO_2 as an insulator film and analyzing its electrical properties. As the ratio of Gd_2O_3 in the dielectric increased, the capacitance density decreased, but the leakage current characteristics were noticeably improved. Furthermore, as a result of analyzing the crystallinity of the Gd-doped ZrO_2 thin film by X-ray diffraction analysis, it was found that Gd doping did not significantly deteriorate the tetragonal crystallinity of ZrO_2.

Acknowledgments This work was supported by the BK21 Plus program. The authors would like to thank SK Trichem for their support and permission to publish this collaborative work.

References [1] W. Jeon, J. Mater. Res. 35, 7 (2020)

8:45am **AA1-TuM-4 Area Selective Co ALD for Highly Reliable ULSI Interconnect System and the Establishment of ALD Process Design Framework**, ***Yukihiro Shimogaki***, The University of Tokyo, Japan **INVITED**

As ULSI becomes more highly integrated, the current density flowing through Cu multilevel interconnects increases, and it has become difficult to ensure device reliability owing to the emergence of wire breakage defects caused by electromigration. In addition, device performance degradation owing to RC delays is a major problem. To solve these issues, it is essential to form a liner layer with a material that exhibits good adhesion to Cu, suppresses electromigration, and crowns the Cu line with a metal cap during the damascene process. It is also important to increase the proportion of Cu in ultrafine Cu interconnects and reduce the effective resistance by employing a thin barrier metal with high Cu diffusion barrier properties.

To address these issues, we have reported that CoW alloy thin films synthesized by ALD have better Cu diffusion barrier properties than existing TaN and higher adhesion to Cu than Ta. We have also shown that Co can be selectively formed on the Cu surface by combining ALD and ALE, and can be used as a metal cap layer.

In this presentation, we report the results of the evaluation of the Cu diffusion barrier properties of CoW films and the development of an AS-ALD process for Co films. To develop an efficient AS-ALD process, we introduce a method to search for novel precursor compounds with appropriate vapor pressures, and a method to estimate and measure the adsorption equilibrium constants of the precursor candidates. We also introduce a method for in situ observation of the incubation cycle by reflectance spectroscopy of the growth surface, and report the results of our investigation of growth conditions and surface treatment methods that exhibit selectivity. These methods are summarized to establish a framework for the ALD process design.

Figure 1 shows the Co film growth on SiO_2 by ALD and ALD/ALE combination. CCTBA (Dicobalt hexacarbonyl tert-butyl-acetylene) was employed as the Co precursor, and a sequential supply of SO_2Cl_2 and HFAC

was used for Co-ALE. Co-ALE was effectively remve the small nuclei formed on the SiO_2 during Co-ALD, which can be used to enhance the selectivity of Co AS-ALD. Figure 2 shows the leakage current of the L/S pattern electrodes with Co-ALD, Co-ALD with HMDS pretreatment, Co-ALD with HMDS pretreatment and ALE combination. Co-ALE and HMDS pretreatments effectively suppressed unwanted nucleation on SiO_2, while Co thin films were selectively grown on the Cu surface.

9:15am **AA1-TuM-6 Atomic Layer Deposition (ALD) of Transition Metal Dichalcogenides (TMDS) Layers as Metal Diffusion Barriers for Back-End-of-Line (BEOL) Applications**, *A. Mane,* Argonne National Laboratory; *S. Katta, J. Morris, C. Phatak,* ***Jeffrey Elam,*** Argonne National Laboratory, USA

The aggressive pursuit of miniaturization in microelectronics has led to a significant reduction in the size of individual device features, consequently boosting device density on chip. This heightened density necessitates more metal interconnect wirings, which, in turn, requires a reduction in wiring dimensions and an increase in the aspect ratio of vias and trenches [https://irds.ieee.org/]. As a result, existing metal lines, typically composed of copper and a liner acting as a diffusion barrier, must undergo proportional shrinking. Scaling down the barrier layer creates a relatively larger volume for copper, effectively keeping resistivity low. However, conventional Ta/TaN thin barriers may exhibit poor performance below 3nm and eventually fail. Therefore, there is substantial interest in exploring new metal diffusion barrier materials, such as two-dimensional Transition Metal Dichalcogenides (2D-TMDs) which hold promise for serving as effective diffusion barriers at smaller thicknesses and layered structured [Deijkers *et al*., Adv. Mater. Interfaces 2023, 10, 2202426].

Here, we present our recent work on thermal low-temperature (200-400ºC) ALD of MX_2 layers including MoS_2, HfS_2, and TaS_2. The ALD of these layers was investigated using in-situ quartz crystal microbalance (QCM) and spectroscopic ellipsometry measurements. Following optimization of the ALD processes, we applied ultrathin layers (4-10nm) of MoS_2, HfS_2, and TaS_2 on Si, SiO_2, and SiN wafers. Subsequently, MOS-type devices were fabricated by depositing 50nm thick copper dots using the sputtering deposition. These MX_2-intigrated MOS devices underwent testing via time-dependent dielectric breakdown (TDDB) measurements. The time-to-breakdown of structures under high electric field stress conditions and failure time were examined as functions of thickness and MX_2 layer chemistries. In addition to TDDB studies, the barrier properties of the MX_2 layers were evaluated using the standard buffer oxide etch (BOE) test. Various types of MX_2-based MOS structures were dipped in a BOE solution, and the etch rate of SiO_2 and SiN was determined and correlated to MX_2 chemistry. This wet etch test study is crucial for evaluating material stability, particularly concerning Cu metal adhesion and chemical stability, which are pertinent during the chemical mechanical planarization (CMP) process. Based on the obtained results, we underscore the potential of ALD for implementing 2D-TMD barriers in BEOL metallization applications.

9:30am **AA1-TuM-7 High-Quality Co Thin Film by Thermal ALD Using CCTBA Precursor by Controlling H_2 Dose**, ***Jun Yamaguchi,*** *N. Sato, A. Tsukune, T. Momose, Y. Shimogaki,* The University of Tokyo, Japan

With the scaling of semiconductor integrated circuits, RC delay and power consumption have increased owing to higher line resistance, and reliability degradation due to electromigration (EM) has become a problem. The use of cobalt (Co) in interconnect layers has attracted attention as a solution to these issues. Co liner, Co cap, and Co interconnects replacing Cu, are expected to address these challenges. For these applications, it is necessary to form high-quality, low-resistance Co ultrathin films uniformly on both the macroscale (entire wafer) and microscale (via, trench). Therefore, the use of atomic layer deposition (ALD) is desirable. From the perspective of substrate damage and step coverage, thermal ALD is preferable to plasma-enhanced ALD. However, the chemical options available for thermal ALD are limited. For instance, while there have been reports of Co-ALD utilizing the $Co(DAD)_2$ precursor,[1] the issue arises from $Co(DAD)_2$ being a solid with a low vapor pressure. In contrast, CCTBA is a highly volatile liquid and an appropriate Co precursor. Therefore, in this study, we focus on the thermal ALD of Co using CCTBA.

Hot-wall ALD equipment was used for Co deposition. CCTBA and H_2 were used as the precursor and reactant, respectively, and N_2 was used as the carrier and purge gases, respectively. CCTBA was vaporized at 45ºC and bubbled with the carrier gas. The chamber temperature was maintained at 100ºC. A sputtered Cu film was used as an underlayer. The composition of the Co film was measured using XPS, and the film thickness was determined using SEM.

Figure 1 shows the growth per cycle (GPC) of the Co film according to the CCTBA supply time. The GPC became saturated after 5 s, and the saturated GPC (0.05 nm/cycle) was smaller than the Co monolayer thickness (0.2 nm). This suggests that the deposition was self-limited via the surface saturation of the adsorbing precursors, which is typical of ALD. Figure 2 shows a cross-sectional SEM image of the Co film deposited on a Si trench structure with an aspect ratio of 8.4. Conformal deposition, a feature of ALD, has been achieved. Figure 3 shows the composition of the Co film versus the H_2 dose. As the H_2 dose increased, the amount of carbon impurities decreased, and the film purity improved. Figure 4 shows the XPS results for the Co film deposited under high H_2 supply conditions. No peaks of C and O, which were present in the CCTBA precursor, were observed, indicating the successful deposition of a high-quality Co film. The Co film resistivity was measured to be 27 μΩ·cm with a thickness of 36 nm.

9:45am **AA1-TuM-8 Improved Properties of Atomic Layer Deposited Ru Films by Providing Additional Reactant for Cu Alternative Interconnects**, ***Jeongha Kim,*** *K. Sang Bok,* Ulsan National Institute of Science and Technology (UNIST), Republic of Korea; *T. Cheon,* Daegu Gyeongbuk Institute of Science & Technology (DGIST), Republic of Korea; *S. Kim,* Ulsan National Institute of Science and Technology (UNIST), Republic of Korea

Ru emerges as a next-generation interconnect materials capable of overcoming the scaling limits encountered with Cu interconnect [1]. Generally, as the deposition temperature increases, the properties of metal thin films deposited by ALD improve due to the grain size increase and impurities reduction by the enhanced chemical reaction. But at deposition temperatures where the precursor thermal stability isn't ensured, its thermal decomposition occurs, leading to degraded in thin film properties such as increased resistivity owing to the significant impurities and retarded grain growth. In this study, a novel ALD-Ru process has been developed, which provides additional reactant followed to obtain high-performance ALD-Ru process capable of maintaining excellent properties, even at temperatures where precursor thermal decomposition happen. Here, a Ru metalorganic precursor, tricarbonyl(trimethylenemethane)ruthenium [$Ru(TMM)(CO)_3$] was used for ALD-Ru. It was reported that by using this precursor, a high-quality film with a very low resistivity (~12.9 μΩ·cm) was obtained in ALD temperature window (260℃)[2]. But, the precursor thermal stability has been kept to ~260℃ and at 275℃, the thermal decomposition of the precursor started and the resistivity of the film deposited at 300 ℃ was again increased due to the incorporation of carbon impurity. In this study, to improve the properties of Ru thin film, ALD-Ru process was done at higher deposition temperature at 310℃. Moreover, to remove contamination of the film resulting from the precursor thermal decomposition, NH_3 has been provided as an additional reactant followed by providing the main counter reactant, O_2, which is called 6-step ALD process (figure 1). Thus, when only O_2 was used (4-step ALD), the GPC was as high as ~2.4 Å/cycle and with the additional injection of NH_3, the GPC decreased to ~1.3 Å/cycle. The resistivity of the film was as high as 20.1 μΩ·cm using a conventional 4-step process but with 6-step process, is was decreased to ~13.6 μΩ·cm. In addition, an increase in peak intensity was confirmed through XRD analysis (figure 2), indicating the improvement of the film crystallinity by 6-step ALD process. An ALD-Ru film with a thickness of 26 nm was obtained with an excellent physical and compositional conformality and nearly 100% step coverage at the hole feature with a high aspect ratio of ~25. In summary, 6-step ALD-Ru process to supply additional reactant followed by the main counter reactant can provide the valuable process option to obtain the high-quality metal film at higher deposition temperature where the precursor thermal decomposition.

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