Atomic Layer Etching
Room Grand Ballroom A-C - Session ALE1-WeM

Si and SiO_2 ALE

Moderators: Prof. Austin Minnich, Caltech, Prof. Gregory N. Parsons, North Carolina State University

8:00am **ALE1-WeM-1 Plasma-Enhanced Atomic Layer Etching for Metals and Dielectric Materials***, **Heeyeop Chae,*** Sungkyunkwan University (SKKU), Republic of Korea **INVITED**

The critical dimensions of semiconductor devices are continuously shrinking with 3D device structure and are approaching to nanometer scale. The demand for dimension control in angstrom level is drastically increasing also in etching processes. Atomic layer etching (ALE) processes are being actively studied and developed for various semiconductor and dielectric materials as well as metals. In this talk, various plasma-enhanced ALE (PEALE) processes will be discussed for isotropic and anisotropic patterning of metals and dielectric materials such as molibdenum, ruthenium, cobalt, titanium nitride, tantalum nitride, halfnium oxide, zirconium oxides. [1-6] Typical ALE processes consist of surface modification step and removal step. For the surface modification, various fluorination, chlorination and oxidation schemes were applied including fluorocarbon deposition, halogenation, oxidation with radicals generated plasmas. For the removal or etching step, various schemes were applied including ion-bomardment, heating, ligand volatilization, ligand exchange, and halogenation. The surface characteristics and requirements of plasma-enhanced ALE will be also discussed.

1) K. Koh, Y. Kim, C.-K. Kim, H. Chae, *J. Vac. Sci. Technol. A*, 36(1), 10B106 (2017)

2) Y. Cho, Y. Kim, S. Kim, H. Chae, *J. Vac. Sci. Technol. A*, 38(2), 022604 (2020)

3) Y. Kim, S. Lee, Y. Cho, S. Kim, H. Chae, *J. Vac. Sci. Technol. A*, 38(2), 022606 (2020)

4) D. Shim, J. Kim, Y. Kim, H. Chae, *J. Vac. Sci. Technol. B.*, 40(2) 022208 (2022)

5) Y. Lee, Y. Kim, J. Son, H. Chae, *J. Vac. Sci. Technol. A.*, 40(2) 022602 (2022)

6) J. Kim, D. Shim, Y. Kim, H. Chae, *J. Vac. Sci. Technol. A.*, 40(3) 032603 (2022)

8:30am **ALE1-WeM-3 Controlling the Hole Profile of High Aspect Ratio Structures in Atomic Layer Etching of SiO2 by Utilizing Dc-Superposition in Capacitively Coupled Plasmas***, **Kang-Yi Lin,** E. Hirsch, P. Wang,* TEL Technology Center, America, LLC, USA

As semiconductor manufacturing advances to nanometer scale processing nodes, the development of contact and via in middle-of-line (MOL) and back-end-of-line (BEOL) schemes continuously shrinks critical dimension (CD) with higher aspect ratio structures. The etching process faces the demand for better control of the profile, including taper angle and the etching selectivity of SiO_2 to the mask and etch stop layer. Conventional approaches, such as continuous-wave plasma, using a mixture of etchants and passivation precursors for selective removal undergo the bottleneck as the feature moves to the nanometer scale. Aspect ratio-dependent transportation impedes the processing window to meet the criteria on etching profile and selectivity. Atomic layer etching (ALE) is an emerging approach that separates the surface functionalization and etching byproduct activation steps to enable selective removal in a self-limited fashion and to mitigate aspect ratio-dependent etching. Our capacitively coupled plasma (CCP) etcher enables a feature that imposes a negative direct current (DC) bias on the top electrode, which attracts ions for sputtering reactions and produces Si deposition and ballistic secondary electrons to the bottom electrode. We studied the effect of DC-superposition (DCS) in CCP under an ALE sequence on the hole profile, including the coating thickness on the substrate, the thickness loss of the mask and etch stop layer, and the etching profile. Other surface characterization methods, including x-ray photoelectron spectroscopy (XPS), were used to understand the surface evolution of each step during the ALE sequence. Experimental results show that DCS can be used to control the etching selectivity and taper angle. The optimal condition delivers a vertical taper angle close to 90° on the etch stop layer with neglectable mask losses. Exploiting DCS in an ALE sequence under CCP offers a novel processing window to improve etching profiles in the nanometer scale feature.

8:45am **ALE1-WeM-4 Damage Analysis of Reactive Ion and Quasi-Atomic Layer Etched Silicon***, A. Karimi,* AlixLabs AB, Sweden*; M. Alabrash,* Lund University, Sweden*; R. Jafari Jam,* AlixLabs AB, Sweden*; D. Lishan,* Plasma-Therm LLC*; H. Aslan, J. Garnæs,* Danish Fundamental Metrology, Denmark*; A. Uvarov,* Plasma-Therm Europe, France*; Y. Ilarionova,* ***Dmitry Suyatin**, J. Sundqvist,* AlixLabs AB, Sweden*; S. Khan,* Danish Fundamental Metrology, Denmark*; I. Maximov,* Lund University, Sweden

Atomic layer etching (ALE) is a cyclic technique based on self-limiting processes, such as reactive gas adsorption and material removal by low-energy ion bombardment. In a typical ALE process Ar^+ ions with energies of 20-60 eV are used to desorb the reaction products, e.g. $SiCl_x$ for the Si ALE. Compared to a corresponding continuous reactive ion etching (RIE), where the ion energies often exceed 100 eV, the ALE should yield less surface damage due to low ion energy and its cyclic nature. However, there are few publications only dealing with studies of the surface damage in ALE.

For Si etching experiments with Cl_2 and Ar as etch gases, we used a commercial Inductively Coupled Plasma RIE Takachi™ tool from Plasma-Therm LLC. The system was operating in a quasi-ALE (Q-ALE) regime with some RIE contribution during the removal step due to residual Cl_2. In order to avoid surface contamination by lithographic masks, a custom-made metal shadow masks were used to protect some Si areas from the Ar^+ ion bombardment. The Kelvin Probe Force Microscopy (KPFM) measurements were then performed both on the reference and the etched places to calculate the contact potential difference (CPD) values for the RIE and Q-ALE samples.

Here we present our results on application of KPFM to evaluate the surface damage of Si for both Cl_2/Ar-based RIE and Q-ALE processes. We used two methods for chlorinating the Si surface: a) molecular chlorination where plasma was only ignited during the Ar^+ etching step and b) plasma chlorination where plasma was ignited during the entire process and pulsed during etching step. The KPFM is used to measure the CPD between the etched Si surface and the tip and this potential difference reflects the surface damage. At the same time, a surface morphology was also characterized in an atomic force microscopy mode. Both the CPD and the surface roughness are used to evaluate the damage after cyclic ALE processes at different RF-bias power. The results were then compared with a sample that had undergone RIE in order to provide a comprehensive evaluation of the impact of the etching process on the surface morphology of the samples.

We present and discuss the CPD and surface roughness data as a function of bias voltages for both RIE and Q-ALE. The experimental results in this study show that the CPD of Si after the Q-ALE processes are in close proximity to the theoretically calculated value. However, if the samples are subjected to continuous RIE with the same parameters, the surface potential deviates significantly from the theoretical value. This may indicate that the Q-ALE process gives a significantly lower damage of Si compared to a standard RIE.

9:00am **ALE1-WeM-5 Atomic Layer Etching of SiO_2 via H_2/SF_6 Plasma and TMA***, **David Catherall,** A. Minnich,* California Institute of Technology

The quality factor of ultrahigh Q silica microdisk resonators has reached values exceeding one billion but remains at around an order of magnitude below intrinsic upper limits due to surface-roughness scattering. Atomic layer etching (ALE) has potential to mitigate this scattering because of its ability to smooth surfaces to sub-nanometer length scales. Here, we report an ALE process for etching of SiO_2 using sequential exposures of TMA and Ar/H_2/SF_6 plasma. The Ar/H_2/SF_6 plasma has been reported to enable in-situ production of HF, enabling HF exposures in the ALE process without the need for an external source of HF vapor. We observe etch rates up to 0.6 Å per cycle and examine the effect on surface roughness. This work advances a process of relevance to ultrahigh Q silica resonators which are fundamental elements of on-chip photonic devices such as frequency combs.

9:15am **ALE1-WeM-6 Learnings and Mitigations of Nonuniformity in Oxide Quasi Ale Applied to Contact Patterning***, **Francois BOULARD**, A. RONCO, N. POSSEME,* CEA/LETI-University Grenoble Alpes, France

Ideal Atomic Layer Etching (ALE) with truly self-limited half cycle offers many advantages to conventional etching processes. The independent control of the modification and the removal steps offers higher etch selectivity, could smooth surfaces, or minimizes the dependence to aspect ratio and wafer location [1]. However, in oxide quasi ALE based on FluoroCarbon (FC) plasma, where a thin FC film is deposited, self-limitation is not obvious. In such circumstance, the return to a pristine surface

between cycles is no longer guaranteed and the Etch Per Cycle (EPC) or surface roughness become very sensitive to process conditions [2]. Moreover, in a throughput perspective, the removal step should be shortened as much as possible, stressing even more the process window. In this paper, we present recent experimental results obtained on 300 mm blanket and contact patterned SiO_2 etch. A multi-frequency capacitively coupled plasma with C_4F_6/Ar chemistry is used. A particular attention is paid to the wafer uniformity of deposition and removal activation. We analyze the impacts of deposition and activation times on the EPC and roughness uniformities. We show how intentional nonuniform deposition and removal half cycles could help to optimize the quasi ALE process. Finally, we apply these understandings on contact etching for Si qubits and FDSOI advanced nodes technologies with stringent soft landing requirements.

[1] K.J. Kanarik, et. al., J. Vac. Sci. Technol. A **35**, 05C302 (2017)

[2] X. Wang, M. Wang, P. Biolsi, and M. J. Kushner, J. Vac. Sci. Technol. A **39**, 033003 (2021)

9:30am **ALE1-WeM-7 Adopting a Low Global Warming Potential Fluorocarbon Precursor (C_6F_6) to Atomic Layer Etching of Sio_2 with Fluorocarbon Plasmas***, **Inho Seong**, Y. You, Y. Lee,* Chungnam National University, Republic of Korea*; G. Yeom,* Sungkyunkwan University, Republic of Korea*; S. You,* Chungnam National University, Republic of Korea

Reducing the greenhouse effect induced in plasma etching with the use of greenhouse gases such as CF_4 and C_4F_8 have been attracting enormous interests in the industry and academia. In SiO_2 atomic layer etching (ALE) with fluorocarbon plasma, we adopt an alternative precursor, C_6F_6, that has been known to have significantly low global warming potential, for gas mixtures with CF_4 and C_4F_8, which is one of the most widely used precursors while has a high GWP. The ALE results obtained with different gas chemistry are monitored by in situ ellipsometry and their ALE characteristics such as self-limiting behaviors are discussed in this paper. We expect this result to provide an opportunity for low global warming potential precursors to be adopted more widely in the etching process.

9:45am **ALE1-WeM-8 Thermal ALE Reactants for Semiconductor Processing***, **Martin McBriarty**,* EMD Electronics

The devices that enable our digital future require clean, selective atomic layer processes to shape their complex 3-D nanoarchitectures. Isotropic ALE is a critical part of this toolkit, but each ALE process will be burdened with strict requirements for high selectivity and low levels of impurities and residues. Bringing such processes online requires ALE reactants that are not only effective, but also safe, sustainable, and readily integrated into the fab. Thermal ALE reactants from EMD Electronics are poised to meet these challenges. Etch performance and selectivity are efficiently tested using high-throughput process screening on 300mm ALE tools, followed by fab-grade physical and electrical characterization. For denser memory devices, we demonstrate ALE methods to shape high-*k* dielectrics which leave minimal residues without requiring the use of corrosive gases. For the interconnects and vias that tie together ever-shrinking transistors, we show ALE processes that selectively and precisely etch metals without compromising their electrical performance. The ALE processes discussed herein can be performed in the vapor phase, without requiring plasma generation, wet etch steps, or corrosive gas facilitization, enabling facile integration of isotropic ALE onto atomic layer processing tools.

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