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ALE and ALD: two biotopes of a kind in atomic-scale processing

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The IRDS 2017 Roadmap catches the scaling challenges faced by the semiconductor industry in the upcoming decades by the overall term "3D Power Scaling" (Fig. 1).[1] In the past scaling era superior material properties and critical dimensions nearing single-digit nanometer values could still be realized by cost-effective technology solutions. As we approach the 3rd scaling era, increased complexity and cost of device fabrication can result in decreased returns for IC manufacturers. Ever more complex device architectures that are fully integrated into vertical intra- and inter-chip concepts require extreme edge placement accuracy, layer conformality and shape fidelity in all processing steps (deposition, lithography, etching).

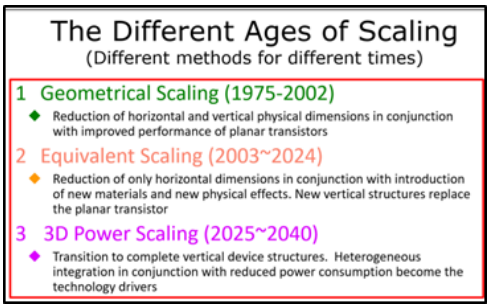

Figure 1: Different scaling ages for device manufacturing (Ref. 1).

In state-of-the-art semiconductor processing we witness an ever-progressing hybridization of individual ALD and ALE process steps into ‘dep-etch’ *supercycling* modes carried out in a single flowchart and a single reactor design, thereby challenging even EUV lithography. This rapid merger finds its grass roots in the close resemblance of the two techniques in terms of cyclic sequential processing, self-limiting surface chemistry and repeated etching or removal of (sub-) monolayers of material. For both ALE and ALD these factors allow for similar process windows that depend on the substrate surface temperature or the kinetic energy of reactants.

In this tutorial more parallels of ALE will be drawn with its more mature and better understood ALD counterpart. Starting with a technical-historical review of dry and reactive ion etching, the key characteristics of ALE will be discussed: the simplest ALE process is composed of two alternating steps, *i.e.* surface modification and (quasi-)monolayer removal. Next, the classification into 1) isotropic (thermal and radical-enhanced) ALE and 2) anisotropic (directional and ion-enhanced) ALE will be treated along the role played by energetic species (radicals, ions in a plasma) in one or two steps with the ions yielding anisotropic profiles (used in FinFET logic and 3D NAND memory), and neutrals and radicals yielding isotropic profiles (used to etch horizontal nanowires in GAA-FETs). Another parallel aspect that may be discussed is the need for (maskless) material-selective processing in both ALE and ALD.

In short, we will identify the similarities and differences between the two process concepts with the aim of bringing common practical insights and recommendations.

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(1) The International Roadmap for Devices and Systems: 2017: More Moore; 2017.