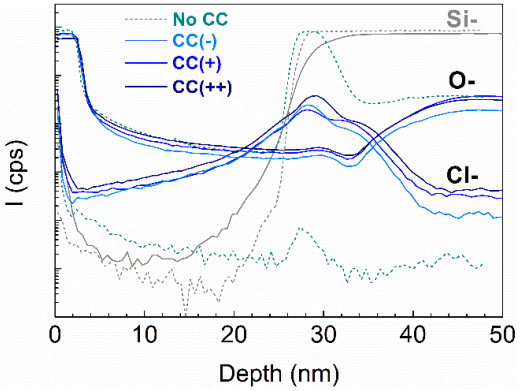

Figure 1: oxide removal and contamination of the interface before and after different number of CC cycles. *(ToF-SIMS)*

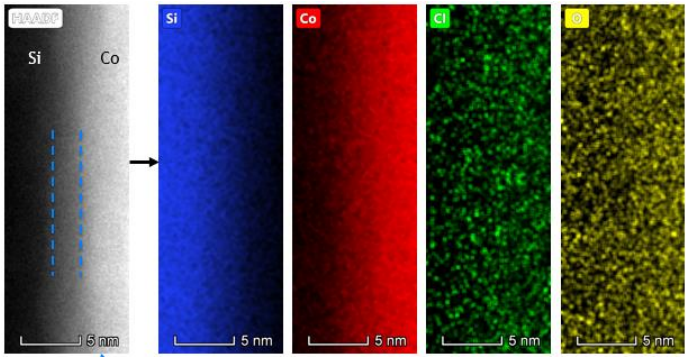

Figure 2: *STEM-EDS* of Si-Co interface. Visible is the Si-Co intermixing layer. O and Cl signal are below the EDS detection limit.

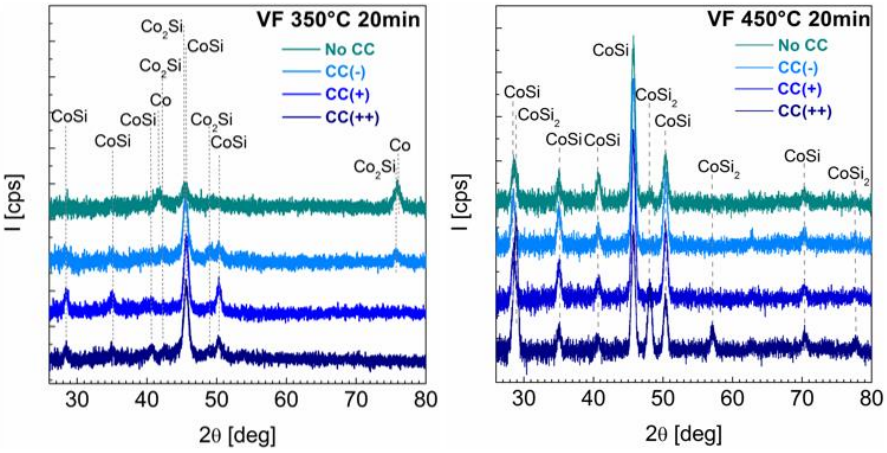

Figure 3: silicide formation as function of CC cycles on Si + PVD Co 30nm, after vacuum annealing at 350°C (CoSi is visible in CC samples only) and 450°C ($CoSi_2$ is visible in CC samples only). *(GI-XRD)*

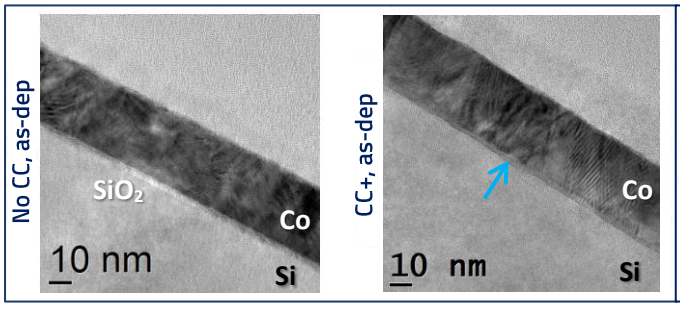

Figure 4: interface of the non-cleaned (native oxide visible) and cleaned Si + PVD Co 30nm (amorphous interface interlayer). *(TEM BF)*

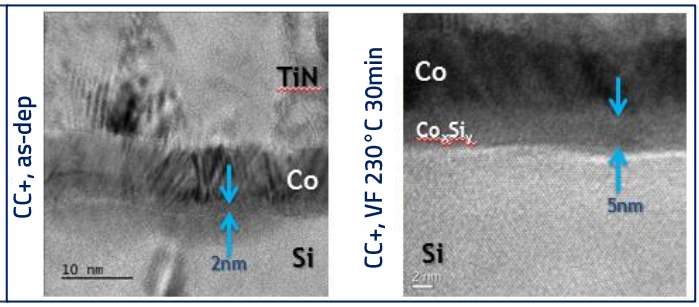

Figure 5: amorphous interface interlayer (CC+) in as-dep and annealed 230°C 30min. Thickness increase visible. *(TEM BF)*

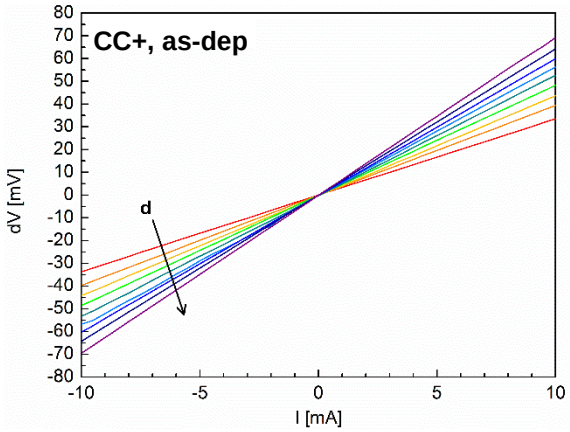

Figure 6: I-V plot of Co/Si-Si/Co TLM contact as function of pad spacing d. The contacts are fully ohmic in the analyzed I range.

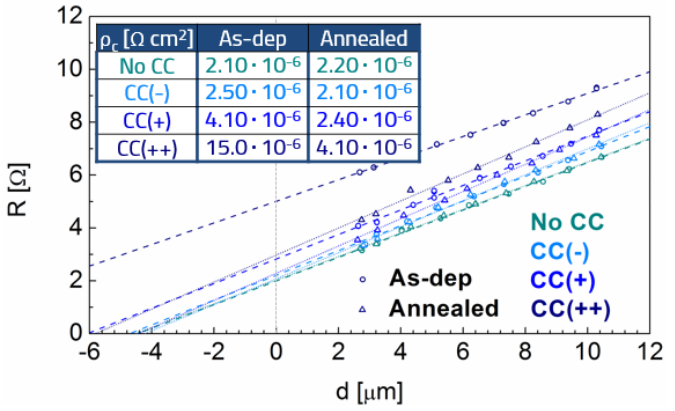

Figure 7: contact resistivity of as-dep and low-T vacuum annealed (230°C 30min) as function of CC cycles. *(Four-point TLM)*