Wednesday Morning, July 24, 2019

ALD Applications

Room Grand Ballroom H-K - Session AA1-WeM

ALD for Memory Applications II

Moderators: Seung Wook Ryu, SK Hynix, Myung Mo Sung, Hanyang University

8:00am **AA1-WeM-1 ALD/ALE Process in Commercially Available Leading-Edge Logic and Memory Devices**, ***Rajesh Krishnamurthy***, TechInsights **INVITED**

In 2018, we saw the introduction of a new generation of logic products, featuring FinFET transistors from Intel with their 10 nm generation microprocessor, followed by 7nm devices from competing foundries, primarily targeting high-end application processors in mobile devices. We also saw memory product manufacturers Samsung, Hynix, Toshiba and Micron introducing 64- or 72- stacked layer 3D-NAND devices, and move into 1x generation DRAM devices.

As a supplier of competitive intelligence to the semiconductor and electronics industries, TechInsights performed structural analyses to examine the features and manufacturing processes of all of these innovative devices.

This presentation will examine some of the different structures we have seen through the evolution of these technologies, in particular 7nm and 10-nm logic, 3D-NAND and DRAM parts, that have been introduced. We will also look at several historical applications of ALD/ALE technology that have been observed through reverse engineering. We will highlight the importance of ALD/ALE process in advanced logic and memory devices. In many cases, the technology could not have advanced without the implementation of ALD technology

8:30am **AA1-WeM-3 Atomic Layer Deposited Crystalline Zinc Oxide for Silver-based Ultra-Steep Threshold Switching Selector**, ***Harrison Sejoon Kim***, *A Sahota, J Mohan, H Hernandez-Arriaga, J Kim,* The University of Texas at Dallas

Along with the growth of emerging non-volatile memory (NVM), developing an outperforming selector is also required to pave the way for realization of neuromorphic networks. Ideally, when cointegrated with the memory element, the role of a selector is to prevent the sneak-current from neighboring devices in a cross-point array [1]. To thrust the emerging NVM at the technological cutting edge, various kinds of selectors have been developed so far [1]. Also, different deposition techniques have been employed to deposit the selector layer. Atomic layer deposition (ALD) provides excellent atomic thickness controllability, thus amongst them, it is the most favorable technique for fabricating the selectors having their switching threshold dependent on the electric field. Electric field dependent conduction mechanism is significant as threshold voltage (V_{th}, voltage that turns on the selector) can be controlled by changing the physical thickness of switching layer. Controllability of V_{th} makes the selector highly compatible with the memory element. Ag or Cu-based threshold switching (TS) selectors are exemplary for the electric field driven selectors, and moreover, they possess superior characteristics over many kinds of the selectors developed so far [2].

In this work, we demonstrate Ag-based TS selectors fabricated with ALD grown crystalline zinc oxide (ZnO) unlike the most prevalent cases where switching layers have been deposited amorphously. The selector device has simple metal-insulator-metal (MIM) structure. Stacked Ag electrodes are assumed to act as the reservoir for providing Ag metal atoms to form metallic filament within insulating ZnO layer (Fig. 1a). As a result, we have obtained robust TS behavior using ALD ZnO with high selectivity (>10^7), ultra-low off-state leakage current (~ pA), high on-state current density (> 0.01 MA/cm^2), and ultra-steep slope (< 10 mV/decade) (Fig. 1b). To suppress cycle-to-cycle variability found in Ag-based TS selectors, we have proposed "Ag delta-doping" concept (Ag-doped ZnO) for minimizing the stochastic issue (Fig. 2). Here, we expect crystalline ZnO would benefit reducing randomness providing better controllability on Ag diffusion (as illustrated in Fig. 2). This will be achieved through a technique so called "super-cycle ALD", followed by further investigation on the reliability of Ag-doped ZnO switching layer.

The authors thank Semiconductor Research Corporation (SRC) for providing financial support in this work.

[1] G. W. Burr *et al.*, *J. Vac. Sci. Technol. B*, vol. 32, no. 4, p. 040802, 2014.

[2] Z. Wang *et al.*, *Adv. Funct. Mater.*, vol. 28, no. 1704862, pp. 1–19, 2018.

8:45am **AA1-WeM-4 ALD Ge-Se-Te OTS Selectors with Controlled Composition for PCM Applications**, ***Valerio Adinolfi***, *L Cheng, R Clarke, S Balatti, K Littau,* Intermolecular, Inc.

The increasing need for faster high-capacity NV-memories have led researchers to explore chalcogenide materials as a solution to fabricate PCM memories and OTS selectors. Memories and selectors are vertically integrated in X-point arrays to produce storage devices. In order to meet the stringent requirements on integration chalcogenide stacks will have to be integrated in 3D structures (as is currently happening for FLASH NANDs). 3D architectures can be enabled exclusively by ALD depositions – providing the necessary conformality and film quality – of the active layers. A limited number of ALD chalcogenide films have been demonstrated but, despite intense efforts, these processes fail in controlling the film composition – fine control over the composition of chalcogenide systems is indispensable for producing performing OTS and PCM devices.

Here we present, for the first time, ALD of binary and ternary films of Ge – Te – Se with controlled composition evaluated in devices as two terminal threshold switches. A unique process involving $HClGe_3$, btms -Te(Se), and Te ethoxide was developed by alternating semiconducting GeTe(Se) and metallic Te/Se layers. Nucleation and growth mechanisms are thoroughly investigated by means of an in-situ ellipsometer. We demonstrate the ability to cover a large part of the ternary triangle plot (see figure attached) by using RBS, XPS, and calibrated XRF. X-SEM and AFM reveal smooth surfaces and compact films. Conformality is assessed by uniformly filling trench structures with a high aspect ratio (40:1).

Finally we electrically characterized $Ge_xTe_ySe_z$ thin films contacted with tungsten and TiN bottom plugs and top contacts (respectively). Different compositions produce dramatically different devices; germanium rich compositions exhibit resistive or PCM behaviors while Te – Se rich compositions produce OTS selectors (see figure attached). DC current-voltage (IV) measurements, transient IVs, and threshold voltage characterizations are performed over a large number of devices and a statistical analysis is presented.

This work shows for the first time ternary ALD chalcogenide films with controllable composition and their electrical operation as memory devices (PCM and OTS); this novel ALD process poses the foundation for the imminent development of chalcogenide based 3D X-point memory arrays.

References:

1) A. Chen, *Solid State Electronics* **2016**, *125*, 25.

2) L. Perniola et al., *IEEE Electron Device Lett.* **2010**, *31*, 488.

3) A. Velea et al., *Scientific Reports* **2017**, *7*, 8103.

4) V. Pore, T. Hatanpaa, M. Ritala, M. Leskela, *J. Am. Chem. Soc.* **2009**, *131*, 3478.

5) T. Gwon, et al., *Chem. Mater.* **2017**, *29*, 8065.

9:00am **AA1-WeM-5 Pulsed CVD of Amorphous GeSe for Application as OTS Selector**, ***Ali Haider***, IMEC, Belgium*; S Deng,* ASM, Belgium*; E Schapmans,* IMEC, Belgium*; J Maes,* ASM, Belgium*; J Girard,* Air Liqude Advanced Materials, France*; G Khalil,* imec*; G Kar, L Goux, R Delhougne,* IMEC*; M Caymax,* IMEC, Belgium

Alongside advances in RRAM structural design to scale down the memory, the problem of sneak currents, which frustrate the accurate reading/writing of data in each cell, remained a critical issue. An attractive approach is to add a selection device operating for example by means of the Ovonic threshold switching (OTS) mechanism to each memory element that suppresses sneak currents through highly nonlinear current-voltage (IV) characteristics. Amorphous germanium selenide (GeSe) is a well-known candidate for OTS selector which so far has only been grown by physical vapor deposition (PVD) for planar RRAM devices. The 3D RRAM approach, which has the advantage of ultra-high storage density with low cost, calls for a uniform and highly conformal deposition technique to deposit this amorphous GeSe selector material on 3D structures.

Here, we report pulsed chemical vapor deposition (CVD) of amorphous GeSe using germanium chloride and alkylsilylselenide precursors. We learned from a study of precursor chemisorption kinetics based on Total Reflection X-ray Fluorescence (TXRF) that both precursors cover the wafer surface only quite slowly. The same measurements also show that Se precursors need Cl sites (from the Ge precursor) for precursor ligand exchange reactions. Further investigation reveals that higher GPC is obtained in pulsed CVD mode (so, no purge steps between the pulses). Based on this basic understanding, we developed a pulsed CVD growth process (GPC=0.3 Å/cycle) of GeSe using $GeCl_2.C_4H_8O_2$ and $(TMS)_2Se$ as Ge

and Se source, respectively. TEM images reveal that ~20 nm grown GeSe layer is amorphous while EDX and RBS measurements revealed stoichiometric GeSe films with traces of Cl impurities. EDX mapping revealed uniform Ge and Se distribution throughout the film. Elastic recoil detection (ERD) measurements show ~5 % carbon inside the grown GeSe film. AFM images show an RMS surface roughness of 1.7-1.9 nm. GeSe grown on 3D test structures showed excellent film conformality.

Currently work is ongoing to apply conformally grown GeSe layers as OTS selector devices in electrical test vehicles. We will report electrical switching and endurance characteristics of conformal, pulsed CVD grown OTS GeSe selector layers and bench mark these with PVD grown GeSe layers.

9:15am **AA1-WeM-6 Thin Film Challenges in 3D NAND Scaling***, **Jessica Kachian**, D Pavlopoulos, D Kioussis,* Intel Corporation **INVITED**

In today's datacentric society, 3D NAND has become a storage architecture of focus through increased bit density, relative to 2D architectures. Continuing bit density increase through 3D NAND scaling requires clever manufacturing strategies, centered on discovery and patterning of target materials. Thin film deposition steps face daunting aspect ratios with unforgiving quality specs. The inherent conformality afforded by ALD makes it an attractive process for 3D NAND. However, many relevant ALD processes do not deliver film quality as-deposited. This talk focuses on general material and patterning requirements for key steps in 3D NAND fabrication and considers how ALD may address these challenges, with attention to target properties towards performance.

Author Index

Bold page numbers indicate presenter