ALD Applications
Room 107-109 - Session AA1-TuM

Memory Applications: RRAM & Neuromorphic, MIM Capacitors

Moderators: Shi-Jin Ding, Fudan University, Jaeyoung Ahn, Samsung Electronics

8:00am **AA1-TuM-1 Using ALD to Engineer Metal/Insulator/Metal Devices***, John Conley, Jr.,* Oregon State University **INVITED**

Simple thin film metal-insulator-metal (MIM) devices find application as capacitors (MIMCAPs) in the back-end-of-line (BEOL) of integrated circuits, as tunnel diodes for optical rectenna based IR energy harvesting, in IR detector arrays, in large area macroelectronics, as building blocks for hot electron transistors, and as selector devices to avoid sneak leakage in resistive memory (RRAM) crossbar arrays. This invited talk will highlight how atomic layer deposition (ALD) insulators, nanolaminates, and metal electrodes can be used to engineer interfaces, materials phases, energy barriers to electron transport, turn-on voltage, and non-linearity and asymmetry of current and capacitance vs. voltage characteristics of MIM and MIIM devices [1-7].

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8:30am **AA1-TuM-3 Impact of Metal Nanocrystal Size and Distribution on Resistive Switching Parameters of Oxide-based Resistive Random Access Memories by Atomic Layer Deposition***, Chang Liu, Y Cao, A Li,* Nanjing University, China

Resistive random access memory (RRAM) devices are promising candidates for nonvolatile-memory (NVM), analog circuits, and neuromorphic applications. The mainstream resistive switching mechanism of RRAM is the formation and rupture of nanoscale conductive filament (CF) inside the insulation layer. However, the random nature of the nucleation and growth of the CFs leads to dispersed resistive switching (RS) parameters, which is a major challenge for oxide-based RRAM applications. The introduction of metal nanocrystals (NCs) has been confirmed to improve electrical uniformity of oxide-based RRAM devices significantly.

In this work, we focused on the impact of metal NCs size and distribution on the RS performances of oxide RRAM by atomic layer deposition (ALD) based on experiment results and theoretical calculation. The dependence of ALD cycles of 50~130 during Pt or $CoPt_x$ NCs growth on the RS parameters of Al_2O_3 memory units has been evaluated systematically. Both memory cells with embedded Pt or $CoPt_x$ NCs show similar trends: with increasing ALD cycles, the forming voltage, set/reset voltage, low resistance state/high resistance state, and resistance ratio firstly decrease and then increase. And in the middle region of about 90 and 100 cycles, the lower RS parameters are obtained with flat change and better RS properties. When ALD cycles exceed a critical value of about 110 to 120, the RS parameters suddenly become large with degraded RS performances due to percolation effect. The impact of metal NCs size and distribution on local electric field strength of RRAM devices has been calculated by using the finite element method. Although all metal NCs with various sizes enhance the electric field strength compared to at the planar region, only metal NCs with proper grain size and areal density (9 nm/6~10×10^{11}/cm^2 in this work) can effectively produce stronger localized electric field at the tip of metal NCs, leading to optimal RS behavior.

Keywords: resistive random access memory, metal nanocrystals, atomic layer deposition, electrical uniformity

8:45am **AA1-TuM-4 Epitaxial Electronic Materials by Atomic Layer Deposition***, Peter J. King, M Vehkamäki, M Ritala, M Leskelä,* University of Helsinki, Finland

ALD has already delivered unparalleled thickness, conformality and composition control in thin films - enabling the continued scaling of MOSFET and DRAM devices to feature sizes previously thought impossible. Additionally, ALD is now a feature defining tool, using the self-aligned layer principle to set the tolerance of device dimension into the nanoscale.

More control is available from the technique in films that are single crystal and registered to the substrate. The advantages here are improved materials properties and better-defined interfaces for improved device properties.

This talk will explore epitaxial layers produced by ALD, and the possibility of growing multi-layer products with the rationale of enabling future electronic devices. Oxide conductor/semiconductor epitaxial multi-layers will be discussed and the advantages and limitations of ALD examined in this context.

Figure 1 presents a TEM measurement of a 8.5 nm $LaNiO_3$ layer deposited on $SrTiO_3$ substrate, demonstrating epitaxial registration after annealing. The film forms anti-phase boundaries to alleviate the strain from the slightly different lattice parameters and lattice types of the integrated films ($LaNIO_3$ is a rhombohedral crystal and forms a pseudocubic epitaxial relationship with the substrate). In this pseudocubic arrangement films are limited to <10 nm in alternating layers, above this thickness the epitaxy is lost and a polycrystalline product results.

9:00am **AA1-TuM-5 Scaling Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ for Back -end of Line Integration***, Jaidah Mohan, S Kim,* The University of Texas at Dallas*; S Summerfelt,* Texas Instruments, USA*; J Kim,* The University of Texas at Dallas

Although ferroelectric random access memory (FRAM) is the most energy efficient memory device (which can operate at <2 V), it has currently reached its scalability limit at the 130 nm node because of two primary reasons: (i) ferroelectric properties could not be demonstrated below 70 nm in conventionally used $Pb(Zr,Ti)O_3$ (PZT) and (ii) It was impossible to demonstrate reliable ferroelectric performance in trenched or stacked capacitors [1-3]. Further, all conventional memory devices are fabricated in the front-end of line making fabrication and scaling more tedious. In the recent years, Ferroelectricity in doped HfO_2 has attracted much attention because of its simplicity in fabrication using atomic layer deposition (ALD), silicon compatibility, ability to scale down <10 nm and its 3D integration capability [1]. Also, the Ferroelectric properties can be obtained at a temperature of 400°C, making it suitable for back-end of line (BEOL) integration.

In this study, the ferroelectric properties of $Hf_{0.5}Zr_{0.5}O_2$ (HZO), deposited using ALD (Cambridge Nanotech Savannah S100) was evaluated, scaling down up to 5 nm. HZO was deposited using TDMA-hafnium ($Hf[N(CH_3)_2]_4$), TDMA-zirconium ($Zr[N(CH_3)_2]_4$), and O_3 as the Hf-precursor, Zr-precursor and oxygen source respectively at 250°C. Blanket TiN (90 nm thick) electrodes were deposited before and after the HZO deposition as it is believed that the stress exhibited by TiN helps HZO to crystallize into a ferroelectric phase [3]. Then, rapid thermal annealing was done at 400°C in an N_2 atmosphere for 60 s to crystallize the HZO films. A conventional photo-lithography/etching process was used to make capacitors of different diameters. After performing the "wake-up" field cycling, polarization-electric field hysteresis and pulse read/write tests were performed to extract the ferroelectric polarization. 10 nm HZO showed very large polarization ($2P_r$ ~ 45 μC/cm^2), saturating at ~1.5 V compared with 7 nm HZO ($2P_r$ ~ 37 μC/cm^2 and V_{sat} ~1.2 V) and 5 nm HZO ($2P_r$ ~ 8 μC/cm^2 and V_{sat} ~1 V). Nevertheless, scaling HZO and reducing the operating voltage lower than 1 V can benefit the development novel FRAM. It was also seen that further annealing of the 5 nm HZO at 450°C increased the $2P_r$ to ~20 μC/cm^2 while maintaining the low saturation voltage. Hence, 5 nm HZO annealed at a low thermal budget (450°C)can be a prospective next generation non-volatile ferroelectric memory with back end of line integration capability.

[1] P. Polakowski et al 6th IEEE International Memory Workshop, Taipei, Taiwan (2014)

[2] S. J. Kim et al 9th IEEE Int. Memory Workshop, Monterey, USA, (2017).

[3] S. J. Kim et al Appl. Phys. Lett., 111, 242901, (2017).

9:15am **AA1-TuM-6 Atomic Layer Deposition Processes for Logic Device Applications**, ***Bong Jin Kuh,*** Samsung Electronics **INVITED**

9:45am **AA1-TuM-8 Effect of ZrO_2 Capping-layer on Ferroelectricity of $Hf_xZr_{1-x}O_2$ Thin Films by ALD using Hf/Zr Cocktail Precursor**, ***Takashi Onaya,*** Meiji University, Japan; *T Nabatame,* National Institute for Materials Science, Japan; *N Sawamoto,* Meiji University, Japan; *A Ohi, N Ikeda, T Chikyow,* National Institute for Materials Science, Japan; *A Ogura,* Meiji University, Japan

Ferroelectric $Hf_xZr_{1-x}O_2$ (HZO) thin films are considered to be promising candidates for future memory device applications such as FeRAM and FeFET, due to its stable ferroelectricity even in extremely thin region (~10 nm) and CMOS compatibility [1]. The HZO films with HfO_2/ZrO_2 nano-laminate structure were typically deposited by the layer-by-layer ALD process [2]. The nano-laminate structure still remains an issue of an ideal ferroelectric HZO film formation. In this study, we investigate the characteristics of the HZO single film deposited by ALD using Hf/Zr cocktail precursor, and discus the effect of a nano-crystallized ALD-ZrO_2 as a capping-layer on the crystallization and ferroelectricity of the HZO films.

The HZO, ZrO_2, and HfO_2 films were deposited on Si/SiO_2 substrates by ALD at 300°C using (Hf/Zr)$[N(C_2H_5)CH_3]_4$ (Hf/Zr = 1/1) cocktail, $(C_5H_5)Zr[N(CH_3)_2]_3$, and $Hf[N(C_2H_5)CH_3]_4$ precursors, respectively, and H_2O gas. The TiN/HZO/ZrO_2/TiN capacitors with a ZrO_2 capping-layer (Cap-ZrO_2) were fabricated as follows: A HZO film was deposited on the TiN bottom-electrode (BE-TiN) by ALD at 300°C. The thickness of the HZO film was varied from 7.5 to 25 nm by changing the number of ALD cycles. Next, a 2-nm-thick ZrO_2 capping-layer was deposited on the HZO film by ALD at 300°C. After that, the annealing was carried out at 600°C for 1 min in a N_2 atmosphere. TiN top-electrodes (TE-TiN) were then fabricated on the ZrO_2 capping-layer by DC sputtering. The TiN/HZO/TiN capacitors (w/o) were also prepared under the same process.

The growth per cycle of the HZO, ZrO_2, and HfO_2 films were estimated to be 0.065, 0.043, and 0.073 nm/cycle, respectively, from the relationship between the number of ALD cycles and the film thickness. The Hf:Zr ratio in the HZO film was estimated by EDS analysis to be 0.43:0.57. Noted that the maximum remanent polarization ($2P_r = P_r^+ - P_r^-$) (23 μC/cm^2) of the Cap-ZrO_2 capacitor with a 10-nm-thick HZO film was approximately 2 times larger than that (12 μC/cm^2) of the w/o capacitor. The $2P_r$ of both capacitors decreased as the HZO thickness increased. Moreover, the ratio of ferroelectric orthorhombic phase of the Cap-ZrO_2 capacitor was significantly larger than that of the w/o capacitor. Therefore, we found that the ZrO_2 capping-layer plays an important role for the HZO formation with ferroelectric orthorhombic phase. Based on these experimental results, a HZO film with superior ferroelectricity can be obtained by using ZrO_2 capping-layer.

[1] M. H. Park et al., Adv. Mater. 27, 1811 (2015).

[2] S. W. Smith et al., Appl. Phys. Lett. 110, 072901 (2017).

Author Index

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