Atomic layer deposition of novel interface layers on III-V channel devices

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III-V compound semiconductors are considered promising transistor channel materials to enable further scaling beyond Si technology due to their high bulk electron mobility values. However, unlike Si, III-V materials have poor quality oxides, and high-k dielectric deposited directly on the III-V surface is problematic due to high density of interface states (D_{it}) and oxide traps. A surface treatment is typically required to passivate the semiconductor surface to minimize the interface states. In addition, a deposited interface layer (IL) is required for the integration with high-k dielectrics to reduce the impact of oxide traps while maintaining a low D_{it}. Although extensive study has been done on searching appropriate IL, commonly investigated high-k metal oxides appear limited in ability to meet the performance requirements for a robust III-V channel transistor.

In this work, a thermal ALD process of a novel material is demonstrated for application as IL in III-V channel devices. The IL material is deposited using a commercially available, hot walled cross flow reactor (ASM Pulsar 3000®). Saturated thickness is demonstrated over a wide range of pulse times in Fig. 1(a) and (b), indicative of operation in the ALD regime. The growth per cycle of is 0.23Å shown in Fig. 1(c). The $In_{0.53}Ga_{0.47}As$ MOSCAPs demonstrate superior D_{it} values $<1x10^{12}$ $cm^{-2}eV^{-1}$, low accumulation dispersion (<1%), and hysteresis (<30 mV) values, extracted from CV characteristic as shown in Fig 1(d). The device performance matches previously published benchmark device metrics for InGaAs channel devices [1]. By employing this novel IL, high performance InGaAs nanowire MOSFETs built on 300 mm silicon wafers is also demonstrated with transconductance reaching 2200 [2].

To further improve the hysteresis or reliability of device, a secondary lanthanum silicate ($La_xSi_{1-x}O$) IL is introduced prior to the deposition of HfO_2 high-k. This lanthanum silicate is deposited by a H_2O-based ALD processes. An ALD master cycle includes a lanthanum oxide sub cycle and silicon oxide sub cycle, shown in Fig. 2(a). Fig. 2(b) shows the growth per master cycle and [Si] content extracted from RI values of bulk films. By using novel IL/lanthanum silicate IL/HfO_2 gate stack, the InGaAs MOSFET demonstrates an excellent electron mobility with a reduced oxide traps meeting the reliability target for 10 years operation [3].

In a summary, we developed novel ALD films for IL application, yielding excellent electrical properties on III-V devices.

[1] M. Radosavljevic et al., IEDM Tech. Dig., 765 (2011)

[2] N. Waldron et al. IEDM Tech. Dig., pp 31.1 (2015)

[3] S. Sioncke et al. submitted to VLSI (2017)

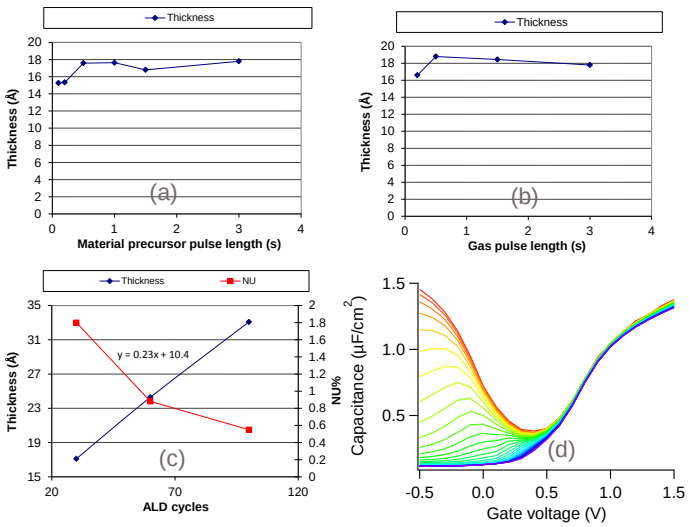

Figure 1. Pulse saturation curves of precursor (a) and (b); and (c) growth rate; and (d) CV characteristic for planar InGaAs MOSCAPs with novel ALD IL

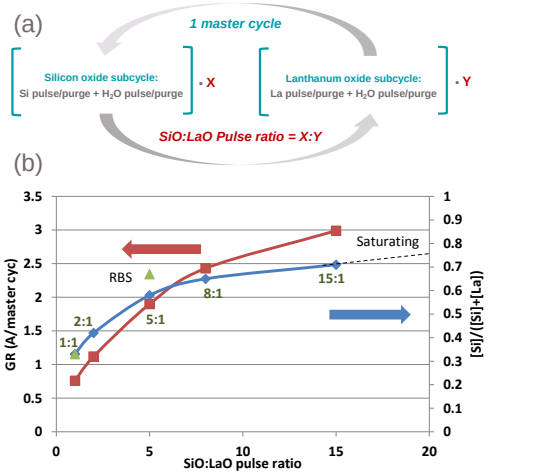

Figure 2. (a) Scheme of lanthanum silicate ALD process; (b)the growth rate and [Si] content of lanthanum silicate process at different pulse ratios