Atomic Layer Processes to Enable the Atomic Scale Era

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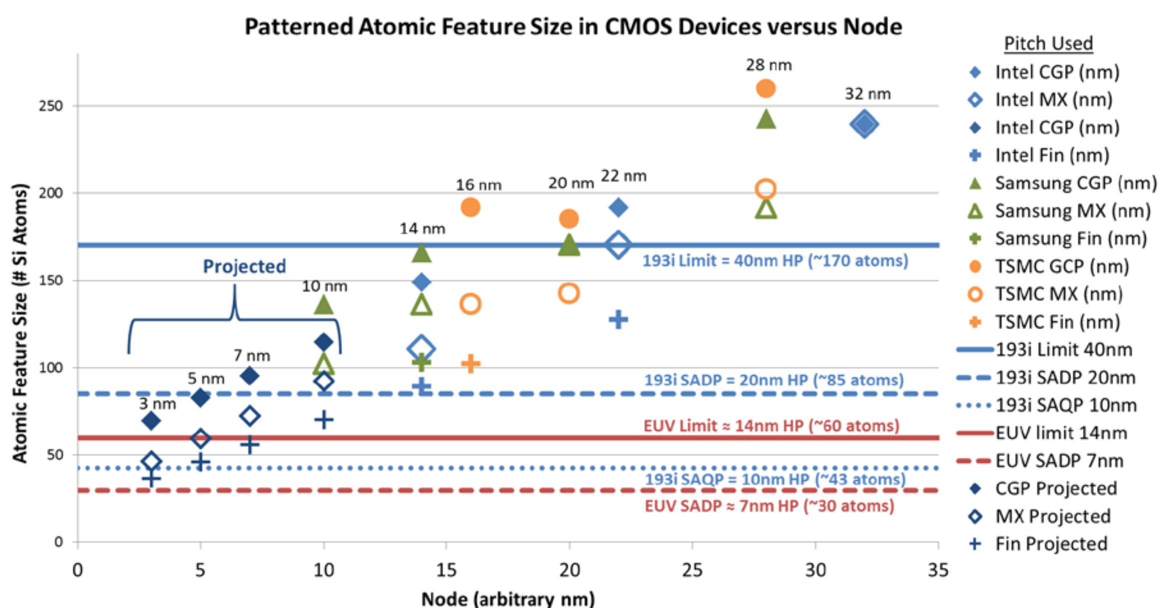
As Figure 1 below demonstrates, the implementation of FinFETs at the 22nm node introduced a new minimum patterned feature size, fin half pitch, into CMOS high volume manufacturing. In addition, the 22nm node marked the initial use of self-aligned multiple patterning for CMOS features, which was required in order to pattern features below the limit of resolution of 193nm immersion (193i) lithography. At the 14nm node Intel's patterned fin feature size fell below 100 atoms in width, marking the beginning of what can be termed the atomic scale era in CMOS manufacturing.[1] Continued scaling is expected to drive all of the critical feature sizes below 100 atoms wide in the near future for CMOS and memory devices as well. Considering features in terms of atoms illuminates a fundamental roadblock to continuing linear scaling: atoms do not scale.

Depositing and etching films used to manufacture atomic scale devices requires atomic level control. Atomic layer deposition and etch (ALD and ALE), including quasi-ALD and quasi-ALE, processes are therefore finding increasingly more use within semiconductor manufacturing. Patterning and aligning features below the lithographic limit requires clever process designs and the inherent control, conformality, and uniformity afforded by ALD and ALE. Likewise, depositing and etching functional films which are in many cases an order of magnitude thinner than the smallest feature sizes can only be controlled using ALD and ALE. Highly selective ALD and ALE processes including area and material selective processes, as well as anisotropic depositions and etches are sought to reduce the reliance and overburden needed for chemical mechanical planarization (CMP) in order to realize bottom up alignment. In this talk we will describe the challenges driving ALD and ALE into manufacturing and provide examples of how we are meeting those challenges with processes that will enable scaling to the 3nm node and beyond.

Figure 1. Historical and Projected Atomic Feature Sizes (half pitch/0.235 nm/Si atom) in CMOS High Volume Manufacturing. Projected feature sizes are based on Intel historical trend



1. S. Natarajan *et al*, IEDM Tech Dig., pp. 71-73, 2014.