Characteristics of Low-k Film at Low Temperature Using SDP System

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As channel length scales further into in the nanometer regime, the parasitic capacitances and series resistance are going to seriously impact the transistor performance. Low-k spacer is a good candidate to minimize parasitic capacitance for high-speed semiconductor applications.

In this study, we present a newly developed SDP ALD/CVD system both rotating the substrate and dividing the source and reactant space area.

We have investigated the characteristics of SiCN and low k SiOCN film by various reactant gas and doping gas and Amine series Si source at low process temperature ranging from 350℃ to 550℃.

We obtained the following results by experiment. SiCN shows the uniformity less than 1% , step coverage 100% at aspect ratio of 10:1, wet etch rate 0.038 Å/sec @100:1 DHF. And Low-k SiOCN shows the uniformity less than 1% , step coverage 100% at aspect ratio of 10:1, wet etch rate 0.1 Å /sec @ 100:1 DHF, Dielectric constant k 4.75. In case of Low-k SiOCN obtained condition that the Leakage Current <1.0E-8A/㎠, Metal oxidation free and Cl Free.

Items	SiCN	SiOCN
Si Source	Amine Series	
Reactant Gas	N_2, NH_3	N2, NH3, N_2O, O_2
k-value	7.41	4.75
Leakage Current (@4MV/cm)	1.0E-7A/cm^2	1.0E-8A/cm^2
Step Coverage (%)	100	100
Wet Etch Rate (Å/min) @100:1 DHF	0.038	0.1
WiW THK Uniformity	<1%	<1%
Chlorine Contamination	Free	Free
Substrate Metal Oxidation	Free	Free