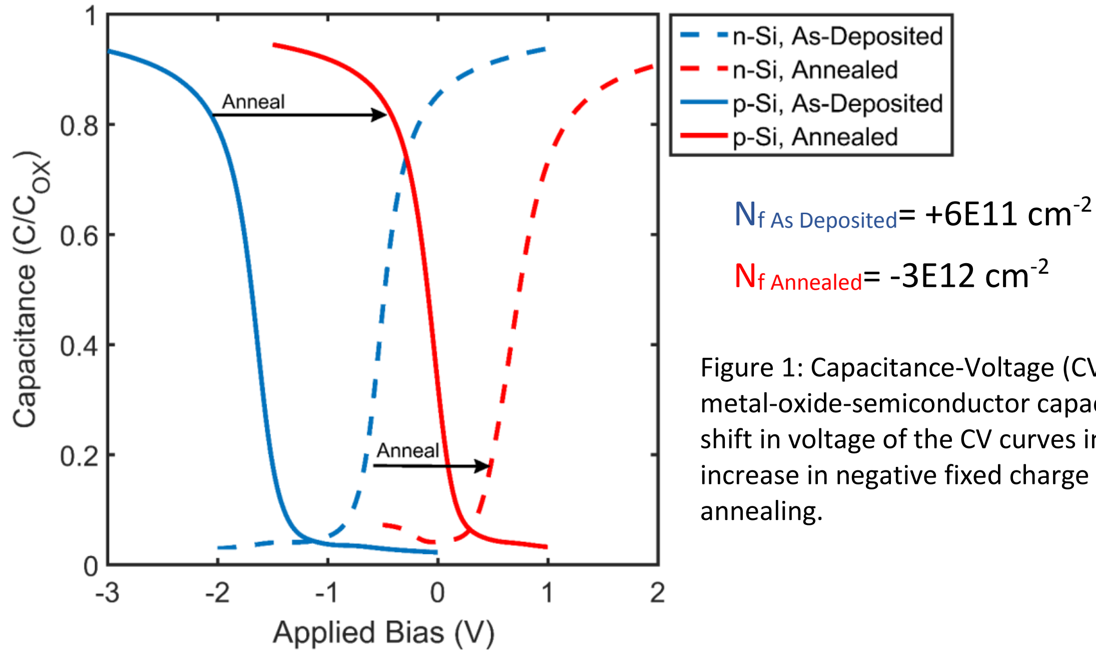

Figure 1: Capacitance-Voltage (CV) data of metal-oxide-semiconductor capacitors. The shift in voltage of the CV curves indicates an increase in negative fixed charge with annealing.

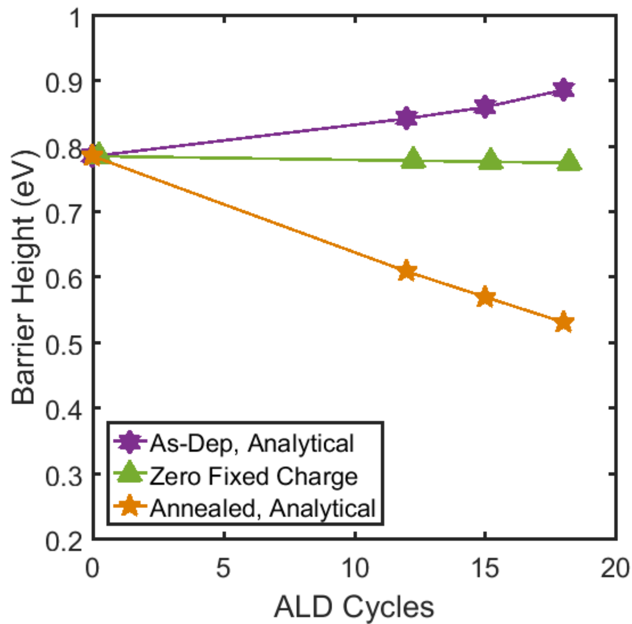

Figure 2: Numerical device physics simulations/ analytical calculations of barrier height for MIS diodes of different oxide thickness. ALD deposition is assumed to be 1 Å/cycle.

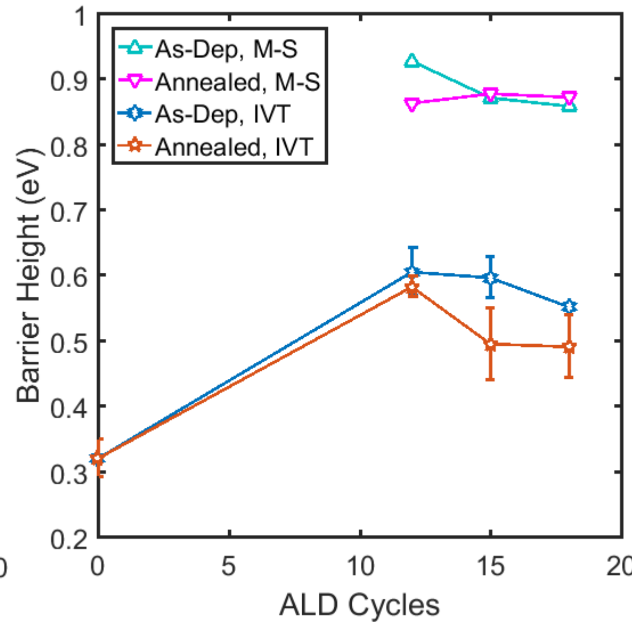

Figure 3: Measured barrier heights for different ALD cycles measured by current-voltage-temperature (IVT) and Mott-Schottky (M-S) methods. The 0 cycle ALD measurement is due to Fermi-level pinning. The As-Dep barrier height measured by IVT and all of the M-S data do not match the simulation/analytical data.