Atomic Layer Etching
Room Plaza D - Session ALE-SuA

Atomic Layer Etching Session I (1:30-3:30 pm) and II (4:00-5:30 pm)

Moderators: Geun Young Yeom, Sungkyunkwan University, Korea, Satyarth Suri, Intel Corporation, Ankur Agarwal, KLA-Tencor

1:30pm **ALE-SuA-1 Atomic Layer Processes to Enable the Atomic Scale Era**, ***Robert Clark***, *K Tapily, J Smith, N Mohanty, S Kal, D Newman, S Consiglio, D O'Meara, K Maekawa, A Mosden, A deVilliers, P Biolsi, T Hurd, C Wajda, G Leusink,* TEL Technology Center, America, LLC **INVITED**

As Figure 1 below demonstrates, the implementation of FinFETs at the 22nm node introduced a new minimum patterned feature size, fin half pitch, into CMOS high volume manufacturing. In addition, the 22nm node marked the initial use of self-aligned multiple patterning for CMOS features, which was required in order to pattern features below the limit of resolution of 193nm immersion (193i) lithography. At the 14nm node Intel's patterned fin feature size fell below 100 atoms in width, marking the beginning of what can be termed the atomic scale era in CMOS manufacturing.[1] Continued scaling is expected to drive all of the critical feature sizes below 100 atoms wide in the near future for CMOS and memory devices as well. Considering features in terms of atoms illuminates a fundamental roadblock to continuing linear scaling: atoms do not scale.

Depositing and etching films used to manufacture atomic scale devices requires atomic level control. Atomic layer deposition and etch (ALD and ALE), including quasi-ALD and quasi-ALE, processes are therefore finding increasingly more use within semiconductor manufacturing. Patterning and aligning features below the lithographic limit requires clever process designs and the inherent control, conformality, and uniformity afforded by ALD and ALE. Likewise, depositing and etching functional films which are in many cases an order of magnitude thinner than the smallest feature sizes can only be controlled using ALD and ALE. Highly selective ALD and ALE processes including area and material selective processes, as well as anisotropic depositions and etches are sought to reduce the reliance and overburden needed for chemical mechanical planarization (CMP) in order to realize bottom up alignment. In this talk we will describe the challenges driving ALD and ALE into manufacturing and provide examples of how we are meeting those challenges with processes that will enable scaling to the 3nm node and beyond.

Figure 1. Historical and Projected Atomic Feature Sizes (half pitch/0.235 nm/Si atom) in CMOS High Volume Manufacturing. Projected feature sizes are based on Intel historical trend

S. Natarajan *et al*, IEDM Tech Dig., pp. 71-73, 2014.

2:00pm **ALE-SuA-3 Thermal Atomic Layer Etching of SiO_2 by a "Conversion-Etch" Mechanism**, *J DuMont, A Marquardt, A Cano,* ***Steven M. George***, University of Colorado

SiO_2 is an important semiconductor material and SiO_2 etching is needed in many steps during semiconductor manufacturing. SiO_2 atomic layer etching (ALE) has been demonstrated earlier using periodic exposures of C_4F_8 plasma synchronized with Ar^+ ion bombardment [1]. In this work, we report a thermal process for SiO_2 ALE based on sequential exposures of trimethylaluminum (TMA) and hydrogen fluoride (HF) at 300°C. The etching mechanism involves the conversion of SiO_2 to Al_2O_3/aluminosilicate by TMA and the subsequent etching by sequential fluorination and ligand-exchange reactions [2].

Ex situ x-ray reflectivity measurements revealed that the etch rate was dependent on reactant pressure. SiO_2 etch rates of 0.027, 0.15, 0.20, and 0.31 Å/cycle at 300°C were observed at reactant pressures of 0.1, 0.5, 1.0 and 4.0 Torr, respectively. *Ex situ* spectroscopic ellipsometry measurements agreed with these etch rates versus reactant pressure. *In situ* Fourier transform infrared (FTIR) spectroscopy investigations also observed SiO_2 etching that was dependent on reactant pressure. The FTIR studies showed that the TMA and HF reactions displayed self-limiting behavior. In addition, the FTIR spectra revealed that an Al_2O_3/aluminosilicate intermediate was present after the TMA exposures.

The Al_2O_3/aluminosilicate intermediate is consistent with a "conversion-etch" mechanism where SiO_2 is converted by TMA to Al_2O_3, aluminosilicates and reduced silicon species. *Ex situ* x-ray photoelectron spectroscopy (XPS) studies confirmed the reduction of silicon species after TMA exposures. Following the conversion reaction, HF can fluorinate the Al_2O_3 and aluminosilicates to species such as AlF_3 and SiO_xF_y. Subsequently, TMA can remove the AlF_3 and SiO_xF_y species by ligand-exchange reactions and then convert additional SiO_2 to Al_2O_3. Other conversion reactions may be helpful to transform various materials that cannot be directly etched to different materials that can be etched using thermal ALE.

[1] D. Metzler, R.L. Bruce, S. Englemann, E.A. Joseph and G.S. Oehrlein, "Fluorocarbon Assisted Atomic Layer Etching of SiO_2 Using Cyclic Ar/C_4F_8 Plasma", *J. Vac. Sci. Technol. A* **32**, 020603 (2014).

[2] Y. Lee, J.W. DuMont and S.M. George, "Trimethylaluminum as the Metal Precursor for the Atomic Layer Etching of Al_2O_3 Using Sequential, Self-Limiting Thermal Reactions", *Chem. Mater.* **28**, 2994 (2016).

2:15pm **ALE-SuA-4 The Challenges and Opportunities in Plasma Etching of Functionally Enhanced Complex Material Systems**, ***Jane Chang***, UCLA **INVITED**

The introduction of new and functionally improved materials into silicon based integrated circuits is a major driver to enable the continued down-scaling of circuit density and performance enhancement in analog, logic, and memory devices. The top-down plasma enhanced reactive ion etching has enabled the advances in integrated circuits over the past five decades; however, as more etch-resistive materials are being introduced into these devices with more complex structures and smaller features, atomic level control and precision is needed in selective removal of these materials. These challenges point to the growing needs of identifying and developing viable etch chemicals and processes that are more effective in patterning complex materials and material systems such as multiferroics, magnetic materials and phase change materials.

In this talk, a generalized approach based on combined thermodynamic assessment and kinetic validation is presented to identify and validate the efficacy of various plasma chemsitries. Specifically, potential reactions between the dominant vapor phase/condensed species at the surface are considered at various temperatures and reactant partial pressures. The volatility of etch product was determined to aid the selection of viable etch chemistry leading to improved etch rate of reactive ion etching process. Based on the thermodynamic screening, viable chemistries are tested experimentally to corroborate the theoretical prediction. Some of the above mentioned material systems such as magnetic materials used in non-volatile memory devices are used as examples to demonstrate the broad applicability of this approach.

2:45pm **ALE-SuA-6 A Novel Process for Atomic Layer Etching of ZnO using Acetylacetone and Remote O_2 Plasma**, ***Alfredo Mameli***, *M Verheijen, A Mackus, W Kessels, F Roozeboom,* Eindhoven University of Technology, Netherlands

Along with the drive for anisotropic processes of Atomic Layer Etching (ALE) there is interest in isotropic counterparts.[1] Therefore, in this work, we demonstrate a novel plasma-assisted ALE process for ZnO which is driven by radicals and therefore anticipated to be isotropic. The process consists of alternating doses of acetylacetone (Hacac) and O_2 plasma, interleaved by Ar purges steps. It is expected that Hacac forms volatile complexes by metal oxide surface chelation (e.g. $Zn(acac)_2$), whereas the O_2 plasma is used as a cleaning step to remove unreactive precursor fragments and to reset the surface for the next etching cycle[2]. This hypothesis is supported by a synergy test of the ALE process, which proved that only the alternated doses of Hacac and O_2 plasma led to etching, whereas neither Hacac, nor O_2 plasma alone resulted in ZnO etching.

The ZnO layer thickness measured by *in-situ* and *ex-situ* ellipsometry was found to decrease linearly with the number of cycles with an etch per cycle (EPC) of ~0.08 nm/cycle. This was corroborated by *ex-situ* FTIR and X-ray diffraction measurements. The ALE process was tested over a range of temperatures between 150 and 300°C. X-ray photoelectron spectroscopy demonstrates that the ZnO stoichiometry is preserved throughout the etching process, without any contamination of the film. The same ALE process was also used for etching other metal oxides such as CuO_x, Al_2O_3 and In_2O_3 yielding EPC values in a range between 0.01 and 0.08 nm/cycle. Furthermore, we demonstrate that this ALE process is selective over SiO_2. This was demonstrated by locally depositing SiO_2 on top of the ZnO to serve as a hard mask for the etching. The selectivity stems from the fact that Hacac does not chemisorb on SiO_2 as demonstrated by independent wet chemistry experiments and FTIR measurements conducted on the ZnO and SiO_2 powders. Finally, we will discuss the influence of the starting material properties, as preliminary investigations indicated that the crystallinity of the material to be etched can affect the EPC.

We believe that this novel plasma assisted-ALE process can be extended to other materials. This chemistry does not involve halogens or halides, which minimizes potential contamination issues. It is important to realize that this ALE chemistry gives selectivity for a different set of materials as compared to halide-based isotropic ALE processes, and therefore represents a valuable addition to the ALE toolbox.

[1]Zywotko, D. R. *et al.*, Chem. Mater. **29**, 1183 (2017)

[2]George, M. A.,*J. Electrochem. Soc.*,**143**, 3257 (1996)

3:00pm **ALE-SuA-7 Determining the Benefits and Limitations of Atomic Layer Etching: A Modeling Investigation**, *C Huard,* University of Michigan*; Y Zhang, S Sriraman, A Paterson,* Lam Research Corp.*;* ***Mark Kushner,*** University of Michigan **INVITED**

Atomic layer etching (ALE) techniques are providing several benefits over conventional etching in maintaining critical dimensions, reducing damage and improving selectivity. During conventional etching, simultaneous synergistic reactions between neutral radicals and ions produce continuous etching. Obtaining the benefits of ALE requires sub-cycles separately consisting of self-limiting reactions – typically passivation and etching. In the ideal case, etching results from a synergy between the ALE sub-cycles, with there being no continuous etching due to simultaneous fluxes of radicals and ions during either cycle. In practice, it is difficult to produce conditions that result in this ideal, self-limited reaction sequence.

In this presentation, results will be discussed from a computational investigation of ALE of silicon in Ar/Cl_2 plasmas and SiO_2 in $Ar/C_4F_8/O_2$ plasmas. Reactor scale simulations using the Hybrid Plasma Equipment Model provide the magnitude, energy and angular distributions of reactant fluxes to a wafer. Feature scale modeling was performed using the 3-dimensional Monte-Carlo Feature Profile Model (MCFPM). An important aspect of modeling ALE is representing the finite thickness of the mixing layer formed by ion bombardment. By tracking particles as they penetrate the solid surface, surface mixing and damage are stochastically modeled in the MCFPM.

Investigations were performed of ALE using ideal and non-ideal conditions to determine the possible benefits and limitations of the ALE process. For ideal conditions, aspect ratio dependent etching (ARDE) could be essentially eliminated and surfaces retained their initial smoothness. Introducing continuous etching pathways during ALE of silicon gave rise to ARDE and increased (or introduced) surface roughness. The impact of these non-idealities were investigated in the ability of ALE to clear the poly-silicon gate etch step in 3D finFETs with varying aspect ratios. Results indicate that the ALE process requires less over-etch time than a similar continuous etch, in spite of the non-ideal reaction pathways that result from using realistic reactant fluxes. The impact of reactor scale non-uniformity of fluxes and ion energy distributions was studied for silicon trench etching, demonstrating the limits of flux and energy non-uniformities that can be remediated by the ALE process. The damage induced by ions during over-etch was studied in silicon and SiO_2 when using ALE to clear 3D contacts after a continuous main etch.

Work was supported by Lam Research Corp., DOE Office of Fusion Energy Science and the National Science Foundation.

4:00pm **ALE-SuA-11 ALE TBD 2**, ***Nitin Ingle,*** Applied Materials **INVITED**

Please submit your abstract to Della Miller, della@avs.org, immediately for inclusion in the program.

4:30pm **ALE-SuA-13 Significant Improvements of CD Uniformity and ARDE in ODL Mask Etching using a Self-limiting Cyclic Etch Approach**, ***Barton Lane,*** *P Ventzek,* Tokyo Electron America*; A Ranjan, V Rastogi,* TEL Technology Center, America, LLC

Critical dimension global and local uniformity nearing a few atom widths in carbon based hard masks is critical for < 7 nm device fabrication. This is very challenging for continuous and pulsed plasma etch processes. We show that a cyclic etching approach leads to striking improvements in both global and local uniformity. The global uniformity refers to uniformity on the scale length of cm and is typically due to variations in plasma and/or radical densities across the wafer; it is measured by the variation in the critical dimension (CD) and is often termed CD uniformity (CDU). Local uniformity refers to the uniformity between nearby features which have different local geometries for example nested versus isolated features and is often termed aspect ratio dependent etching (ARDE). We consider the etch of a patterned hydrocarbon spin cast film (ODL) using an argon/oxygen chemistry. Such films are used as part of a trilayer mask system and are common in patterning applications. The cyclic scheme breaks the etch into its two fundamental steps: an oxidation step in which oxygen moieties are introduced into the polymer matrix; and a volatilization step in which the oxidized moieties are detached from the polymer matrix. Using pairs of coupons placed in regions of a test bed reactor with significantly different plasma and neutral species densities, we show that using the cyclic scheme relative to a continuous process, that the CDU can be improved significantly. The underlying reasons for the improvement are the self-limiting nature of both the oxidation and the volatilization steps in the etch process. We show by "*in situ* OES SIMS" experiments how this self-limitation process occurs in the case of the argon and oxygen chemistry. In brief, the oxygen containing step leads to an oxidized layer; the argon only sputter step volatilizes this oxidized layer and then rapidly creates a carbonized, hydrogen depleted layer which has a low etch rate following its initial formation. The self-limitation in the argon sputter step is due to the low etch rate of this carbonized layer. In the oxygen step the high density of the carbonized layer prevents the diffusion of oxidizing species into the polymer interior after an initial saturation of the surface with oxidized moieties. This leads to a self-limiting process for a lean chemistry (low oxidizing species density).

4:45pm **ALE-SuA-14 Nanometer-Scale III-V 3D MOSFETs**, ***Jesus del Alamo,*** *W Lu, X Zhao, D Choi, A Vardi,* MIT **INVITED**

In the last few years, as Si electronics faces mounting difficulties to maintain its historical scaling path, transistors based on III-V compound semiconductors have emerged as a credible alternative. To get to this point, fundamental technical problems had to be solved though there are still many challenges that need to be addressed before the first non-Si CMOS technology becomes a reality. Among them, harnessing the outstanding electron transport properties of InGaAs, the leading n-channel material candidate, towards a high-performance nanoscale MOSFET has proven difficult. Introducing a new material system is not the only challenge, scalability to sub-10 nm gate dimensions also demands a new 3D transistor geometry. InGaAs FinFETs, Trigate MOSFETs and Nanowire MOSFETs have all been demonstrated but their performance is still lagging Si. At MIT, we have focused in the last few years in developing etching technology for high aspect ratio III-V fins and nanowire to support the development of sub-10 nm 3D MOSFETs. We have demonstrated fins as narrow as 15 nm with an aspect ratio of ~10 and nanowires with a diameter of 20 nm and an aspect ratio of ~11. Following RIE, our nanowires and fins are trimmed using digital etch. This consists of an oxidation step in O2 plasma and an oxide removal step in a diluted acid. By separating both steps, the process is self-limiting and yields a very precise etching rate (in our case, about ~1 nm/cycle). We have also shown that digital etch improves the sidewall electrical characteristics. Using digital etch, we have been able to demonstrate InGaAs FinFETs with 7 nm wide fins and record transconductance characteristics. Regarding nanowires, the high surface tension of water-based acid makes it impossible to reduce their diameter below ~12 nm. Beyond this dimension, the nanowires collapse due to strong mechanical forces during digital etch and the yield of the process quickly drops to zero. We have recently solved this problem by using alcohol-based acids with a much lower surface tension. Using the same oxidation step, the new technique shows an etch rate of 1 nm/cycle, identical to the conventional approach. Sub-10 nm fins and nanowires with a high yield and mechanical stability have been achieved. InGaAs nanowires with diameter of 5 nm and an aspect ratio > 40 have been demonstrated. The new technique has also been successfully applied to InGaSb-based heterostructures, the first demonstration of digital etch in this material system. Vertical InGaAs nanowire gate-all-around MOSFETs with a subthreshold swing of 70 mV/dec at V_{DS} = 50 mV have been obtained demonstrating the good interfacial quality that the new technique provides.

5:15pm **ALE-SuA-16 Atomic Layer Etch Processes Developed in an ICP/RIE Etching System for Etching III-V Compound Semiconductor Materials**, ***Xu Li,*** *Y Fu, S Peralagu, S Cho, K Floros, D Hemakumara, M Smith,* University of Glasgow, UK*; I Guiney,* University of Cambridge, UK*; D Moran,* University of Glasgow, UK*; C Humphreys,* University of Cambridge, UK*; I Thayne,* University of Glasgow, UK

In this work, we compare several atomic layer etch (ALE) processes developed in an ICP/RIE etching system based on Cl_2/Ar and HBr/Ar chemistries for etching GaN, AlGaN, InAlN, InGaAs, and InGaSb. These processes will be very important in the realisation of various energy efficient electronic devices including gate recess etching of GaN power transistors, and controlled sidewall cleaning in InGaAs and GaInSb finfets and nanowires for continued logic scaling.

Investigations were carried out in an Oxford Instrument PlasmaLab Inductively Coupled Plasma (ICP) etching system with repeat loop function. The etching chemistry is based on the self-limited formation of Al, Ga, In, Sb chlorides or bromides on the semiconductor surface as a consequence of exposure in Cl_2 or HBr gases or plasmas during the sample surface modification step of the ALE cycle. This is followed by an Ar plasma selective surface layer removal step at an optimized RF power level at which the Ar plasma only removes the surface chlorides or bromides. Reducing the power of the Ar plasma process is vital to minimizing damage to the underlying III-V materials.

A parametric exploration of the process space showed that an ALE window can be established for both the Cl_2 and HBr based processes by simply flowing the reactive gas across the sample surface – it is not necessary to establish a plasma of the reactive gases. Further, that given the response time of mass flow controllers on the etch tool, a minimum gas flow time of 2s was required to ensure process stability and repeatability. This relatively long dwell time meant that the reactive gases had to be diluted with Ar – optimal dilution ratios were found to be 8:42 Cl_2:Ar and 6:44 HBr:Ar; all at chamber pressures of 50 mTorr, total gas flow of 50 sccm, and platform temperature of 20°C. Ultimately, processes to produce repeatable removal rates of 0.13 nm/cycle were obtained in this way. Experiments also showed that the Cl_2 and HBr processes modified the III-V surface layers differently, due to the relative volatilities of the chlorine and bromine compounds formed on the III-V material surfaces. The Cl-based chemistry required an Ar plasma RF power of 33 W for surface layer removal, whereas this could be reduced to 20 W for the HBr-based chemistry. This is very important in reducing process induced damage. Experiments showed that there no observable change in either the electron mobility or channel carrier concentration in an AlGaN/GaN HEMT for RF power levels for the Ar plasma of less than 25 W at a chamber pressure of 50 mTorr; therefore an HBr-based ALE process is most appropriate for use in the realization of III-V devices.

5:30pm **ALE-SuA-17 Enhanced Thermal ALE of Aluminum Oxide Combined with ALD for UV Optical Applications***, **John Hennessy**,* Jet Propulsion Laboratory, California Institute of Technology*; C Moore,* University of Colorado - Boulder*; K Balasubramanian, A Jewell,* Jet Propulsion Laboratory, California Institute of Technology*; K France,* University of Colorado - Boulder*; S Nikzad,* Jet Propulsion Laboratory, California Institute of Technology

This work demonstrates the development of a thermal atomic layer etching procedure using alternating exposures of trimethylaluminum and anhydrous hydrogen fluoride that is used to controllably etch aluminum oxide. This ALE process is modified relative to existing HF-based methods through the use of an intermediate reaction during TMA exposure with a conditioning film of lithium fluoride. This is shown to enhance the loss of fluorine surface species and results in conformal layer-by-layer etching of deposited aluminum oxide films. The Al_2O_3 etch rate was measured over a temperature range of 225 to 300 °C, and was observed to increase from 0.8 to 1.2 Å per ALE cycle at a fixed HF exposure. The variation in etch rate is the result of increased surface fluorination during HF exposure, and the extent of this fluorination has a clear dependence on the total effective HF dose delivered per ALE cycle. Nevertheless, the process is shown to be scalable to large area substrates with a post-etch uniformity of better than 2% measured on 125 mm diameter wafers.

This ALE process utilizes the same chemistry previously demonstrated in the ALD of AlF_3 thin films, and can therefore be used to remove the surface oxide from metallic aluminum and replace it with thin fluoride layers in order to improve the performance of ultraviolet aluminum optical components by reducing the loss associated with the oxide layer. We will discuss how this approach has applications in the development of vacuum UV instruments, in next-generation UV mirrors for JPL-NASA astrophysics missions, and in enhancing the performance of nanostructured metallic Al for UV plasmonic applications. The efficacy of the technique is demonstrated by measurements of UV reflectance on evaporated aluminum films undergoing the described ALE + ALD procedure. We will present material characterization by x-ray photoelectron spectroscopy, ellipsometry, and atomic force microscopy; and we will discuss the mechanism associated with the etch enhancement produced by co-reaction with LiF.

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